
Test Quality Tools Speed Development of High Quality In-Circuit Test Programs

Case Study for Using Teradyne's Test Quality Toolset

Application Overview

This Application Brief documents the results of running a suite of automated test quality software tools, available on the Teradyne TestStation In-Circuit Testers, on a Printed Circuit Board.

The software that was used is part of Teradyne's TestStation Test Quality tool suite and consists of the following independent but integrated functions.

AutoDebug

The AutoDebug tool automatically debugs failing or marginal test program measurements using debug commands contained in an autodebug command file. AutoDebug runs until the test measurement passes specific test quality criteria. The debug commands, as well as the test quality criteria, can be customized by the test operator.

Adjust Limits

The Adjust Limits tool attempts to improve analog test measurements by shifting and/or widening test limits to meet specific test quality criteria. This tool adjusts measurement limits to minimize the chances for false failures.

Analyze

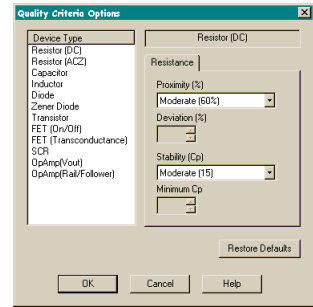
The Analyze tool analyzes the test program and generates a report showing the overall test fault coverage, defects that cannot be detected, and failing and marginal test measurements.

Optimize Throughput

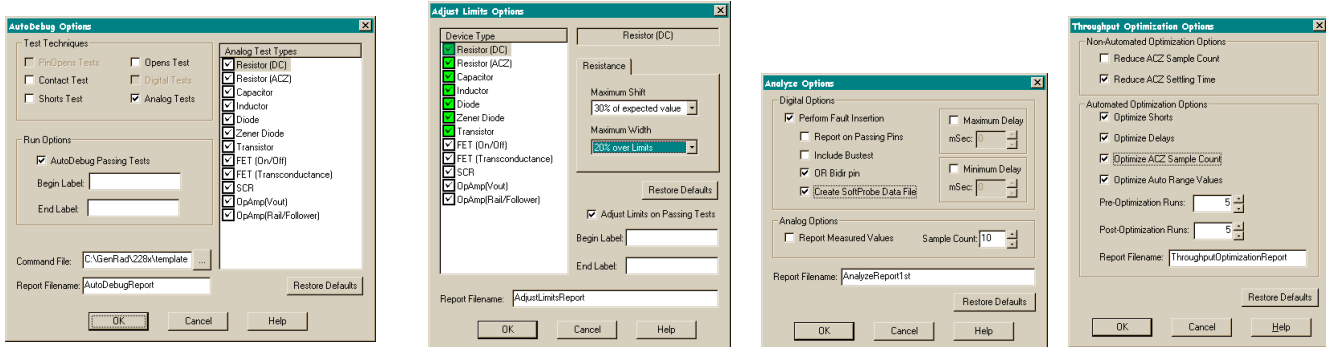
The Optimize Throughput tool attempts to improve test throughput by adjusting test algorithms, settling times, instrument delays, and instrument ranges.

Set Quality Criteria

The Quality Criteria Options are used by each of the above tools to set criteria for test measurement Proximity and Stability. Proximity specifies how close the measurement must be to its expected value and Stability (measured using CP) specifies how much the measurement will be allowed to vary from run to run. The higher the specified CP value, the less the measurement may vary.



AutoDebug, Adjust Limits, Analyze, and Optimize Option Windows



Hardware / Software Requirements

The Test Quality toolset tools will run on any Teradyne TestStation or legacy 228X test system that is running software version 5.6.1 or greater.

Application Example

The test case that was selected to run using the Test Quality tools was a complex dual processor PCB with multiple memory caches, clock filters, SRAM Port, and high frequency stitching CAPS.

The test program for this complex PCB was developed by an EMS service provider and was being run by the OEM in their manufacturing environment.

PCB Statistics

Below are some general statistics about the PCB:

- **Dimensions:** 16.5 x 11 inches
- **Components:** 3034
- **Nets:** 4027
- **Technology:**
 - ◆ 6 different power voltages (5V, 2.5V, 3V, 5V, 12V, 48V DC)
 - ◆ 6 DC-DC Regulators
 - ◆ 54 Digital Logic components including Alpha CPUs, IBM BGAs, SRAM, Xilinx PLD
 - ◆ 5 Cache Daughter Cards
 - ◆ 965 Resistors
 - ◆ 332 Resistor Packs

- ◆ 1578 Capacitors
 - ◆ 11 Inductors
- Fixture Statistics

Below are some general statistics about the test fixture:

- **Manufacturer:** Southwest Test
- **Design Type:** Single Sided Wireless with no board flex
- **Probe Count:** 4015 (2410 100mil, 820 75mil, 785 50mil)
- **Weight:** 110 pounds
- **Capacitive Probes:** 6

Strategy

Since the test fixture and program had already been debugged and was being used to test PCBs in manufacturing, it was decided to only use the Test Quality Analyze, Adjust Limits, and Optimize Throughput tools. These tools would report test program fault coverage and reliability, identify and correct marginal tests, and optimize for maximum test throughput.

The results of using these tools on this program, fixture, and PCB are documented below.

Analyze

Figure 1 shows the results of running the Analyze tool on the PCB test program. The summary shows that there were no failing analog or digital tests. 2046 of the 2414 recognized analog test measurements passed the defined test quality criteria. However, 368 analog test measurements were deemed marginal because they did not pass the defined Stability and Proximity metrics which were set to their default values of 15 and 60%. These marginal tests could potentially cause false failures to be reported if not corrected.

The digital summary shows that the powered digital vector tests can detect 92.7% of the possible faults on the device signal pins. Specific details about where fault coverage is lacking and which tests do not meet the quality criteria were written to the Analyze Report file. This file can be reviewed by test operators to quickly see how the test program fault coverage and reliability can be improved.

The Analyze tool took approximately 70 minutes to run, but most of this time was spent running the digital fault insertion algorithms on large (greater than 500 pins) digital ICs. If this option was turned off, Analyze would run in significantly less time.

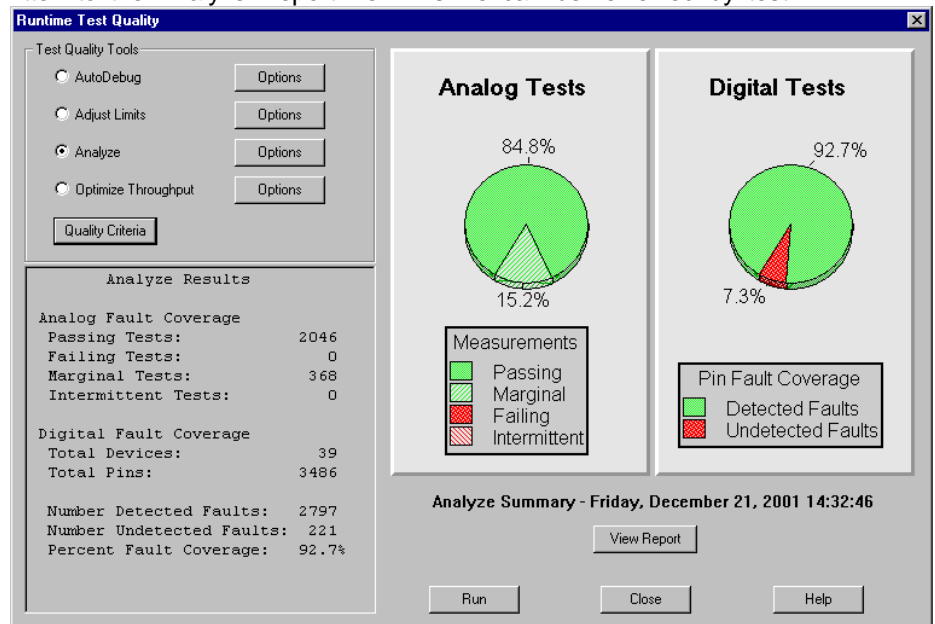


Figure 1: Analyze Summary Window

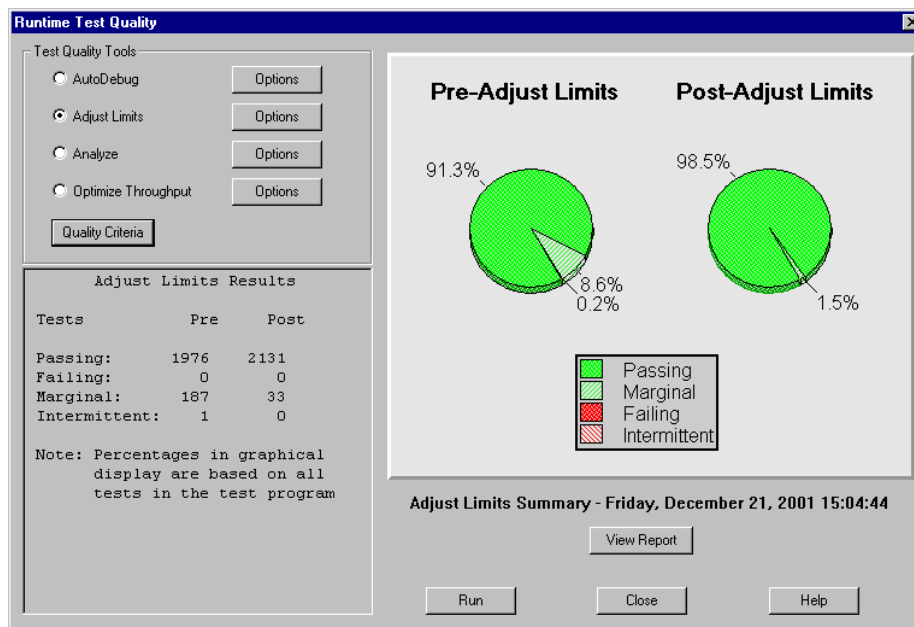
Adjust Limits

The Adjust Limits test quality tool was used next to reduce the number of marginal analog test measurements by shifting or widening the test limits. Shifting the test limits helps fix test measurements that are marginal because they are too close either to the low or high measurement limit. Widening the test limits helps fix tests that are marginal because they have a wide variation.

Figure 2 shows the summary of running the Adjust Limits tool on the PCB. It took 20 minutes to run and reduced the number of marginal tests to just 33 analog measurements. Specific details about what was done to each test to improve stability and proximity can be found in the Adjust Limits Report.

The quality criterion that was used by the Adjust Limits tool was a Maximum Shift adjustment of 30% of Expected Value, and a Maximum Width Adjustment of 20% over limits.

Figure 2: Adjust Limits Summary Window



Optimize

Once satisfied with the test program fault coverage and test measurement reliability, the Optimize test quality tool was run to maximize the test throughput of the test program. The Optimize software looks for alternative Shorts test algorithms, different instrument autorange settings, and reduced delay and settling times to improve the test program throughput.

The Optimizer software took 30 minutes to run and Figure 3 shows that it was able to reduce the overall time required to test this PCB from 51 seconds down to 39 seconds, a 24% throughput enhancement. The Optimizer Report shows that the test throughput improvements were the result of reduced test delay times, settling times, and fewer instrument range changes.

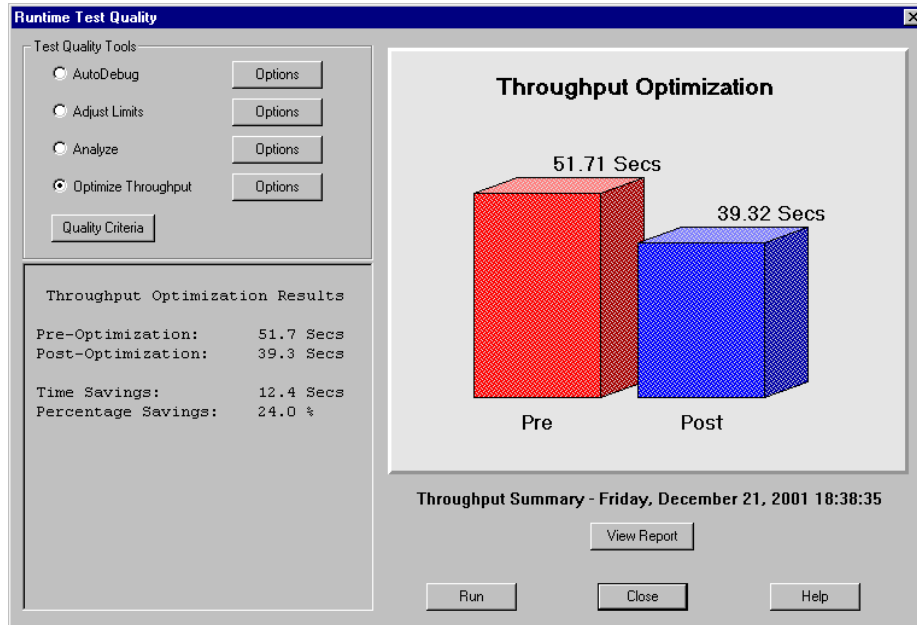


Figure 3: Optimize Summary Window

Conclusion

This application example shows that the Test Quality tools that are standard with the TestStation software can be used to gain insight about the quality of the test program, and significantly improve test program measurement reliability and test throughput. These Test Quality tools, combined with the new automatic ICA calibration feature, will make it easier for manufacturers to create test programs that can be transported to different sites and different test equipment with minimal debug effort.

Additional Information

For more information on Teradyne's Test Quality tools refer to the TestStation Test & Debug manual.