From Design to Production — GSO Tools
>>> GSO — YOUR SOURCE FOR THE TOOLS* YOU NEED

Whether it’s for —

DIB Design or Code Development or Code/Silicon Debug or Production

>>> We have a tool for you!

Designing a DIB?
Simplify your work with –
- Remote Start Switch
- SEDana

Debugging Code/Silicon?
Simplify your work with –
- DIBViewer
- Remote Start Switch
- Runtime Toolset
- SEDana

Developing Code?
Simplify your work with –
- ASCII Utils
- IG-XL Utils
- Remote Start Switch
- SEDana
- WaveWizard

In Production?
Simplify your work with –
- DtWire
- Remote Start Switch
- SEDana
- SMART

* Glossary of Tools is on page 2.
ASCII Utils – Improves test program development, productivity and reusability. One Add-In for all releases of IG-XL – supports J750/FLEX/UltraFLEX. Enhanced Export Workbook (save program to ASCII). Automatically generates test program batch file for loading ASCII-based programs. It is independent of revision control software. Supports sub program modularity.

DIBViewer – Makes the job of locating components and signals while debugging test programs and repairing DIBs faster and easier on today’s high density, multisite DIBs. It works without detailed knowledge of the design tools or actual DIB design. Its easy-to-use interface and full feature capabilities make it simple to search for a component or signal and zoom to the location in both the schematic and layout simultaneously. It saves time; searching is done in seconds vs. minutes and you no longer need to search the PDFs of layout schematic and plots. It has layering, zooming and panning – all the viewing features you need for DIB information during a debug session.

DtWire – A licensed product which can be installed on a Windows-based system; it does not require IG-XL and can operate on all test systems. It creates customized sequences or roadmaps that transfer data to a remote location at a user-defined schedule using DtWire’s advanced GUI, step-by-step wizard or one of the templates. It sets up multiple roadmaps to carry out a variety of actions at predefined times and allows users to develop Filters to customize actions.

IG-XL Utils – This tool, comprised of all the bug fixes and enhancements for all the IG-XL utilities developed by Teradyne engineers, is now under SVN revision control and compiles for both FLEX and UltraFLEX IG-XL software.

Remote Start Switch – A mechanical switch designed to run an engineering-loaded test program on all IG-XL-based testers (including FLEX, microFLEX, UltraFLEX and J750), the Remote Start Switch can be used for test program engineering development and manual lot testing for test data collection.

Runtime Toolset – A fast and easy debug toolset. Some features include the capability to execute a full run of the test program without stopping on existing VB breakpoints, easily perform a trap on fail, error or alarm (needed to set an IGXLEventHandler), jump from one pattern start to the next automatically, and see at a glance all the results of a pinlistdata (without navigating into the structure in the watch window).

SEDana – A tool for quick and practical data analysis developed from the perspective of the test applications, product, and quality assurance engineers. It enables real-time monitoring of test results and statistics, supports ATDF, STDF, and many other formats, and enables engineers to create comprehensive reports with its extensive tables, plots, and reporting options.

SMART – Aids in integrating product, planning, production and debugging IG-XL. The System Management/Analysis and Regression Tool is scalable, providing quicker responses on system configuration, hardware availability and loading needs as well as program configuration requirements and individual test resources mapping. It is a hardware management, system reconfiguration tool which is scalable to a new system and instruments. It has a built-in IG-LatoR (IG-XL + translator) tool for IG-XL test program analysis.

WaveWizard – A pattern conversion program with an automatic tool for generating ATE programs from the designer’s simulation data. It generates a test program according to the device spec, avoiding the inherent problems that exist when trying to force an event-driven simulation into a constrained ATE test program. Uses common engineering tools such as timing diagrams, logic-analyzer type waveforms, and tabular datasheet terms. Inputs are the drawn timing diagrams, the Verilog VCD file, EVCD, STIL, and WGL; outputs are the test program files to run the tester.

**NEED SUPPORT?**

Email gso.centralengineering@teradyne.com

**WANT MORE INFORMATION?**

http://teradynegso.com