

UPCOMING WEB SEMINAR

WPI Presents Analysis of Damage to Low-Voltage CMOS Devices During In-Circuit Test

Vectorless ICT - Best Practice Techniques

When: Wednesday, Aug 23, 2006 at 9:00 AM and 3:00 PM (EST)

This 45-minute live seminar will explain how to apply the latest vectorless in-circuit test technologies to identify open pins and test grounded metal BGA packages with fewer false passes. Join Teradyne Chief Scientist, Anthony Suto, as he also unveils best-practice approaches to testing power grounds on connectors and making accurate frequency and amplitude measurements. Learn how to automatically detect and compensate for source loading and switch to lower frequencies to increase pin coverage. Become knowledgeable in the use new test algorithms and modes of operation to maximize accuracy and noise performance. Please join us as we go in-depth on Teradyne's most advanced tool for vectorless ICT, FrameScan FX.

Register today at <https://teradyne-atd-events.webex.com>

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