TERADYNE

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eTeraView

The e-newsletter of Teradyne's Assembly Test Division

UPCOMING WEB SEMINAR

Avoiding Damage to Low-Voltage CMOS Devices During In-Circuit Test

When: Wednesday, July 26, 2006 at 9:00 AM and 3:00 PM (EST).

Join Teradyne's staff scientist, Anthony Suto, as he describes practical ICT and pin electronics technologies needed to avoid over-voltage stress, a condition that can cause significant damage to the gate oxide of a low-voltage IC through a mechanism called Time Dependent Dielectric Breakdown (TDDB). This 30-minute seminar is for assembly test engineers who must accurately evaluate assembled PCB functionality without risking the ultralow-voltage logic devices aboard.

Register today at https://teradyne-atd-events.webex.com

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