

Analog Functional Testing at the Board and Box Level

Stephen Fairbanks
Assembly Test Division
Teradyne, Inc.



Analog Functional Testing at the Board and Box Level

Stephen Fairbanks
Assembly Test Division
Teradyne Inc.
North Reading Mass.

Phone (978)370-2700 Email Steve.Fairbanks@Teradyne.com

Abstract

Today's automatic test system architecture is based on a Shared Resource technique. These test resources are allocated throughout the test system in order to provide the highest possible asset availability at that test systems interface. As a result, test requirements and test development efforts are bounded by the availability of these limited tester resources.

Digital test developers can take full advantage of system modeling tools to provide the high quality functional tests that mission critical hardware demands. Analog test developers are faced with the challenge of allocating test resources during TPS development. This limits the ability of the engineer to match the high level of operational / functional testing that is required to adequately test a Unit Under test as it is actually used in the Next Higher Assembly. This paper will explore the possibilities of providing a solution for this problem.

Introduction

Today's automatic test system architecture is based on an instrument allocation technique that is designed to both distribute and share resources. Specialized test resources are allocated throughout the test system in order to provide the highest possible asset availability at the test system's interface. As a result, test requirements and test development are bounded by the availability of these specialized tester resources.

With the advent of high performance, high density and general purpose digital subsystems, the implications of sharing digital resources have been minimized. The result to the test development process is a luxury of saving time and effort since the task of allocating stimulus and measurement assets is all but eliminated. Digital test developers can take full advantage of system modeling tools to provide the high quality functional tests that mission critical hardware demands.

On the other hand, Analog test developers are faced with the challenge of allocating precious few test resources during TPS development. The possibility of utilizing high density analog stimulus and measurement assets is close to nil. Also, the capability to match the high level of operational/functional testing that digital TPS developers enjoy is unfortunately not readily available for analog test developers. This paper will explore the possibilities of providing a solution for this problem.

Shared Resource Architecture

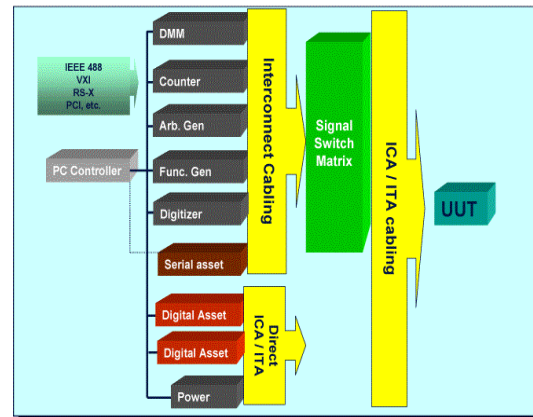


Figure 1. Shared Resource Test System

The concept of shared resources is bounded by the common implementation technique of using a summation of individual single purpose instrumentation within a test system framework. The distribution of these individual instruments within this framework is solved using either internal multipoint constructs or by presenting the developer with the opportunity to statically route any desired assets through customized interface designs. Either implementation will solve the problem of signal allocation for signal simulation at the unit under test (UUT) boundaries. The capabilities of signal simulation are now limited by both the characteristics of the individual instrumentation and that of each allocation path.

Figure 1. outlines the main components with a typical shared resource framework. A common controller accesses the test assets through a single bus or a combination of standard communications buses. HP-IB, VME/VXI/MXI, Serial communications, PCI/C-PCI, SCSI etc., are all used as control gateways that form the central architectural feature of the test system. Common functions form the core subsystems for the test system. These would include a Stimulus sub-system, a Measurement sub-system and a Control/Communications sub-system. Each one of these subsystems is created using a collection of instrumentation that may be distributed across most of the test system I/O using a matrix or muxing scheme. For this discussion, a matrix is thought of as a switching scheme that lets any number of inputs connect to any or all of the outputs at one time. A Mux is a switching scheme that only one input can be switched to one output at one time.

Functional Testing

Functional testing has the honor of having many definitions, all of which basically mean; testing something in a fashion that emulates what that thing does in it's true environment. For this discussion, lets define testing as the means to ensure the health of a unit and functional testing as a means to ensure the operational health of a unit.

In an ideal world, the unit under test (UUT) would first be completely qualified through design and prototype verification. This verification process would then be fine tuned to provide the most effective test qualification procedures. These procedures would ensure the operability of the unit during it's real life use. A test system would then be crafted to fulfill the requirements outlined in those verification procedures. Or an existing test system could be used if it was determined to be appropriate. The functional tests now become implementation of these procedures on some test system. Now let's take a closer look at this test development procedure.

The functional test development life cycle can be broken up into a series of stages; system design, prototype verification, production test and depot repair. Each one of these stages may target very different functional aspects of the UUT and each stage will have its share of problems for the

functional test developer. It's also common that each stage has it's own test requirements that the test developer must act against. For the moment, let's take a look at the first stage, design.

Assuming that the unit had a design modeling stage, the initial verification would be done in the simulation process. After product synthesis, verification involves both operational issues and process proofing for manufacture. The operational design verification stage typically involves either a system emulation on lab equipment and/or a hot mockup station. Both of these techniques tend to have the affect of forcing the design verification into functional segments. Each segment or cluster of activity is isolated into partitions. Proving singular functional partitions leads to a test technique called Sensitized Path Testing (SPT).

Sensitized Path Testing

SPT is a very common method of testing the functions of a UUT. Since each major function can be tested individually, it has the benefit of requiring a minimal amount of test equipment. As each individual function is being tested, the test equipment need only change it's access points for stimulus and measure. In order to automate this process, a matrix or mux is be used to dynamically route the I/O of the test equipment as each new functional partition is being tested.

Each stage of a functional test traditionally takes advantage of the benefits found with SPT. While this process gives you a high degree of flexibility and maximizes the utilization of your equipment, it does have its share of draw backs.

At one or many points in the functional test life cycle, the test requirement definitions are defined. The method of using SPT in the design stage is one example. Here, the test requirement definitions, based on functional test partition, are created using standard lab testing techniques. The process needed to test each partition are selected, characterized recorded and so on. At the end of this process, the requirements definition would be declared complete. One functional partition strategy that usually escapes this process is the full transfer of the system environment. The result is test requirement that may be missing the means to ensure the operational health of the UUT.

Since it is part of SPT to isolate functional segments, providing real time signal simulation for a full system emulation test can be a problem, if not impossible. It may be adequate to verify the individual functions within a unit, but verifying the unit under actual operating conditions is the goal of a functional test. Real time signal emulation across the entire UUT is usually impractical within a shared resource system architecture.

Functional I/O is at a premium in systems using SPT. Given that, your test development will require switching scheme to get those individual test assets around. This extra step introduces a serial effect into the test execution and adds precious test time into the process. Throughput naturally suffers since the test time can become a slave to tester resources, rather than unit delay time.

Today's test system architecture of shared resources, using SPT, is a consequence of the difficulties in providing highly parallel analog sub-systems. A more parallel approach than that available today would both eliminate these process delays and provide a means to do real time signal emulation.

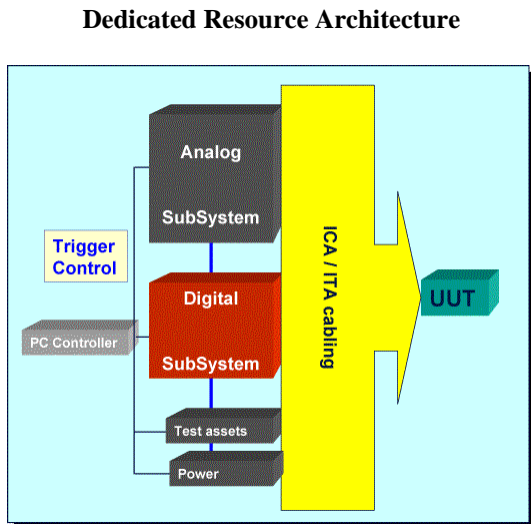


Figure 2. Dedicated Resource Test System

In order to provide a highly parallel test capability, every test system functional capability should be available on every test system I/O at all times. This requires an architecture breakthrough that provides dedicated functional testing resources on every test interface pin beyond what matrices and multiplexers can provide. This innovation in

analog testing capabilities would provide an option to SPT. Since no capabilities would be shared from pin to pin, these capabilities can be considered Dedicated. This leads to a new form of test system design called Dedicated Resource System Architecture (DRSA).

DRSA requires that each test system I/O channel be able to provide the full testing capability without sharing resources from another I/O pin to do it. This would, for instance, require that every I/O pin needed to perform a safe-to-turn-on test, be able to measure resistance to ground. In other words, one ohm meter per I/O pin. As your overall test requirements grow, so too do the per I/O capability requirements. Supporting this style architecture would require a very large integration effort not only at the sub-system level, but also at the test system I/O channel level.

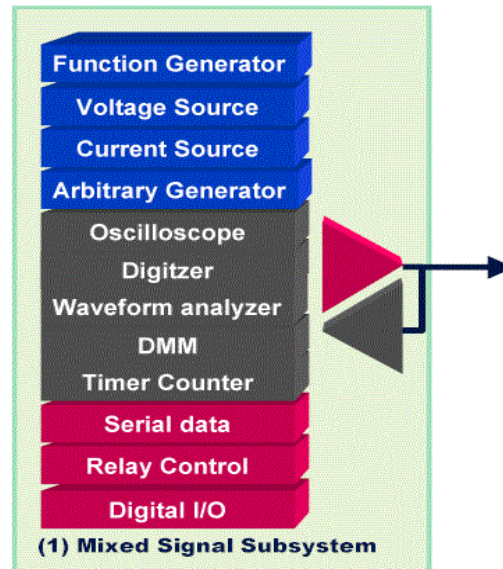


Figure 4. Single DRSA Test I/O pin

Within this sub-system, every test access channel would have the I/O capability that would be expected from a fully functional test interface.

Teradyne's AI-710 Analog Testing Sub-system does exactly this. This is the industry's first mixed signal sub-system on a card designed specifically to address the requirements for real time signal simulation at functional test.

AI-710 Analog Sub-System

A single AI-710 VXI-C sized card provides 32 fully functional, DRSA style I/O channels. Each

channel has 6 dedicated and independent instruments. Each instrument is autonomous and can be activated at will, while being connected to a unique system triggering scheme.

Each AI-710 card contains 32 independent channels for a total of 192 instruments in a single VXI-C size Slot. Figure 3 shows the instruments available on every channel. With an analog subsystem design using a card like the AI-710, test system configurations can now be determined by matching the total I/O requirement with the number of DRSA style tester channels.

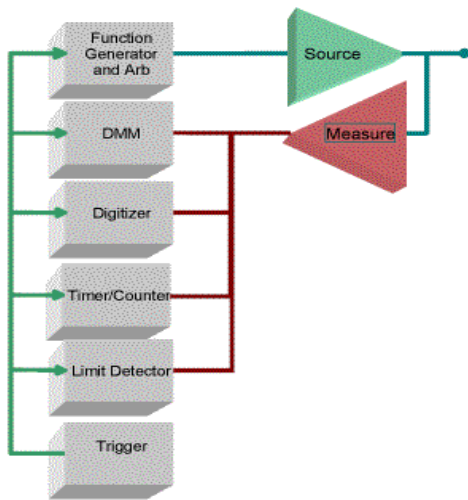


Figure 3. AI-710 Tester Per Pin

Many changes in test technology had to take place in order for this breakthrough to occur. Incredible advances in packaging technologies for analog components have led to huge integration benefits for both DACs and ADCs. DACs are now one tenth the size, one tenth the power and one tenth the cost as they were just 5 years ago. Slower ADCs are approaching the low end speed of “Fast” ADCs, at one fifth the size and cost, with one fiftieth of the power requirement. New low-voltage mixed signal manufacturing processes have provided a step function change in analog designs. Integrated mixed signal functions like 32 bit sine wave generation now costs much less and are housed in very tiny packages.

The result is a highly integrated analog testing subsystem architecture that provides tester per pin resources and matrix free test system designs.

Real Time Parallel Testing

Real time signal emulation in a full system functional transfer would be achieved in a highly parallel way with a test system designed with dedicated resources as its analog core. Implementing DRSA in test system designs take full advantage of high performance digital subsystems and now highly parallel analog test subsystems like the AI-710.

Test requirements definitions can now include system level signal simulation in full operational transfer testing. Functional test partitioning can still be implemented where required for legacy compatibility or test system re-hosting efforts.

Each level of testing will benefit from increased test system throughput, now gated by UUT delay and communications. The SPT process typically involves not only a serial test flow, but also a matrix/mux allocation effort that naturally comes with an extra programming step. This step, repeated for each test entry, may now be eliminated since DRSA would no longer require complicated allocation schemes.

Logistics and maintenance cycles can now be set at the subsystem level with streamlined Sparing and easy-swap repairs. Minimizing the total number of unique test system assets benefits all aspects of test system ownership.

Conclusions

Functional test development and definition based on a DRSA design helps solve the challenge of incomplete requirements definition and removes the bottlenecks associated with a muxed tester scheme.

DRSA requires that all of your testing resources are available at every test pin, all the time. This high level of resource availability is now possible with the emergence of new, highly parallel, mixed signal testing technology.

Sensitized path testing can be augmented or replaced by sensitized operational testing. Both board and assembly level testing can now take advantage of this test technique to increase throughput and enhance functional coverage, while providing the best possible test solution.

Teradyne Inc.
Assembly Test Division
600 Riverpark Dr.
North Reading, MA 01864
Tel. 978-370-2700
Fax. 978-370-1440

000C048-1200