Optimizing Test Strategies During PCB Design For Boards With Limited ICT Access

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ABSTRACT

Engineers have used past experience or subjective preference as a means for assigning test strategies to new products without analyzing the benefits and weaknesses of various different test approaches in a quantitative manner. DFT software tools that enable testability analysis during board design allow test engineers to work concurrently with designers. Case study results demonstrate that coverage predicted by DFT software is realistic when compared to actual fault coverage achieved in production. Using DFT software during PCB design to model the fault coverage of different test strategies and make ICT access tradeoffs can significantly reduce cost and improve quality. Defect capture rates more than doubled when using alternate test strategies and production line beat rates varied significantly depending on the test strategy chosen. When DFT software enables these decisions early in the product life cycle, both OEMs and EMS providers can win by driving cost reductions through the entire product life cycle from NPI through manufacturing and warranty.

Key Words : AXI, AOI, DFT, DFM, DFx, Test Strategy, ICT, Limited Test Access

INTRODUCTION

In today's world of electronics manufacturing there is ever increasing pressure to reduce cost, increase quality and shorten time to market. Test strategies can be leveraged to provide organizations with strategic advantage by improving the efficiency and delivered quality of business processes. Test can be used to gain advantage in a competitive environment by driving cost reductions and improved performance through the entire product lifecycle from design, through new product introduction (NPI), manufacturing and warranty. The return on investment (ROI) of an effective test strategy can total 3 weeks improved time to market and over one million dollars[1].

Electronics manufacturers have a multitude of issues to consider when designing process test strategies[2] for their PCBAs; a variety of tools including automated optical inspection (AOI), automated X-ray inspection (AXI), flying probe test (FPT) and in-circuit test (ICT) are available. Each of these technologies has its own fault coverage and performance characteristics that users must evaluate against their fault spectrum and performance goals before determining their test strategy. Engineers must balance tradeoffs between operating costs, capital costs, fault coverage, throughput, diagnostic resolution, immediacy of process feedback and long-term product reliability when considering an optimal test strategy. The loss of physical test access adds another dimension of complexity to the problem for many modern PCBAs; determining fault coverage and prioritizing the nets that require physical access in a boundary scan and digital test environment is a difficult challenge. By using multiple test techniques in a complementary or distributed manner, manufacturers can best achieve their performance goals.

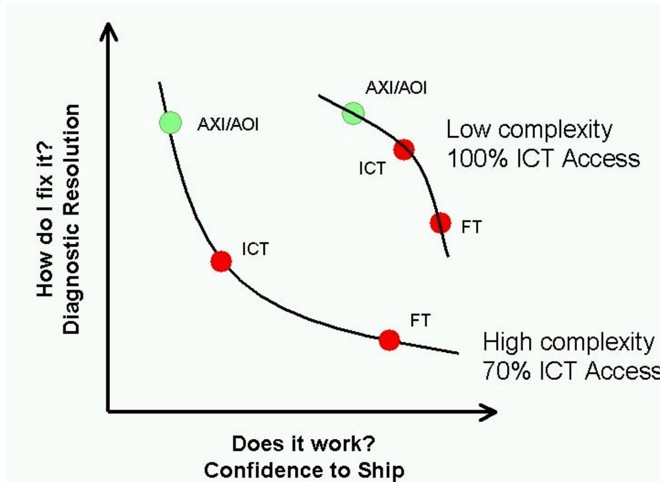
Which tools should be used in a distributed test strategy? What is the fault coverage provided by each of the test techniques? How should tests be distributed to achieve performance goals? What is the correct balance of complementary vs. overlapping test coverage? Which nodes require test access and which do not? What are the risks/gaps in my optimized test strategy? These are the questions engineers are trying to answer in our modern manufacturing test environment. Furthermore, increasing time to market pressures mandate that we plan for and optimize our test strategies early in PCB design, before manufacture. This paper investigates the need for distributed test solutions; case study data illustrates how design for test (DFT) software can be used to optimize test strategies during PCB design to achieve a balance between test coverage and test cost.

A DISTRIBUTED TEST STRATEGY IS REQUIRED

No single test technique is a "cure-all" for all test challenges; each has its own strengths and weaknesses and needs to be evaluated as a possible solution within the overall test plan. Although automated inspection methods are capable of finding defects closer to source for quick debug and repair, they do not ensure confidence in product function, as do ICT digital and functional test methods.

Figure 1: Diagnostic Resolution. Test methods with higher diagnostic resolution exhibit lower cost of debug, higher process improvement value (because root cause is more clearly identified) and require lower skill level debug operators. Functional test methods, although generally poor in their diagnostic resolution, provide confidence in product

function not attained via other methods. Differences are amplified when ICT access is limited. A combined test approach is required – especially for boards with limited ICT access.



Different methods of test also vary in their fault coverage as demonstrated by Figure 2 below.
A distributed test strategy that addresses the right balance of requirements like diagnostic resolution, fault coverage, test access, test development time, skill levels and training costs, uptime and utilization, cost and throughput will most often deliver optimum results for a particular PCBA.

THE NEED FOR DFT AND TEST STRATEGY SOFTWARE

How does one develop best practice distributed test strategies? Since each test approach has varying performance levels along many different characteristics (Figure 1: Diagnostic Resolution and Figure 2: Fault Coverage provide just two examples of the eight criterion listed above), one can easily imagine the evaluation matrix growing to unmanageable proportions. When solving a problem with so many dimensions of complexity, a modern software analysis approach is required. Without an effective quantitative analysis approach, the high number of choices and convoluted, overlapping characteristics of the different test methods would make optimizing a test strategy very difficult and time consuming and lead to questionable results at best.

Figure 2: Fault Coverage of Various Test/Inspect Systems

	HVI	API	AOI	AXI	FPT	MDA	ICT	FT
Solder Short	◆	◆	◆	✓	◆	◆	◆	◆
Solder Open	✗	◆	◆	✓	◆	◆	◆	◆
Solder Reliability	✗	◆	◆	✓	✗	✗	✗	✗
Wrong Part	✗	✗	✓	✗	✓	✓	✓	◆
Missing Part	◆	✗	✓	✓	✓	✓	✓	◆
Bad Part	✗	✗	✗	✗	✗	◆	◆	✓
Mis-oriented	◆	✗	✓	◆	✓	✓	✓	◆
Functional Reliability	✗	✗	✗	✗	✗	✗	✗	✓

Assumptions: 5000 Nodes, 25000 solder joints, 80% node access by ICT&MDA, 10 BGA devices on board.

Legend:

✗ Low or No Coverage

◆ Medium Coverage

✓ Good Coverage

HVI – Human Visual Inspection
API – Automated Paste Inspection
AOI – Automated Optical Inspection
AXI – Automated X-ray Inspection
FPT – Flying Probe Test
MDA – Manufacturing Defect Analyzer
ICT – In Circuit Test
FT – Functional Test

In the past, engineers often chose test strategies based on past experience or subjective preference. ICT

combined with human visual inspection has been an effective test strategy for many years and has been arbitrarily applied to many PCBAs without analysis as to a more optimum test strategy using the new methodologies available today. Modern PCBAs in today's cost and time competitive environment require that we achieve a more optimal test performance for each board on a case-by-case basis. This requires software modeling of test coverage for specific component reference designator pins in order to address issues of lost ICT access, fault coverage of library device models and the particular performance requirements of individual boards. Each PCBA will have a unique fault spectrum; if the software is used to design a test strategy with the fault spectrum of the board in mind, a more optimum and complete result will be achieved.

A critical requirement for PCBAs with limited ICT access is testability analysis during design, prior to manufacturing. Test optimization and modeling software that enables testability analysis prior to the layout routing stage of PCB design will deliver fewer design iterations, faster time to market, improved fault coverage and lower production test costs.

DFX FOR BOARDS WITH LIMITED ICT ACCESS

DFx[3] is a key focus area for OEMs today because it accelerates time to market and time to volume, reduces manufacturing costs and lowers defect rates. By verifying PCB designs with a manufacturing "rules checker", non-conformances that could severely impact production quality levels can be easily rectified. Similarly, effective testability analysis during design can significantly improve production test performance.

DFT software enables test engineers to work concurrently with designers; they can predict the fault spectrum, plan test strategies, understand fault coverage and test access tradeoffs prior to the layout routing stage of PCB design. Some types of software predict a fault spectrum for every pin, component and signal on the board, and thereby identify which test pads will provide the greatest test coverage. By listing the test pads that provide the greatest test coverage in descending order, designers can make intelligent decisions on which test pads should be provided on boards with limited access. The bottom line is fewer design iterations, fewer snags, and improved manufacturing test performance at lower cost. Furthermore, if the software models the fault coverage provided by each machine in the distributed test plan, it can identify which test pads can be removed because of overlapping fault coverage from other test stages.

DFT SOFTWARE TEST COVERAGE ANALYSIS

Analog, Digital and Boundary Scan Model Libraries

The software must use analog, digital and boundary scan model libraries for accurate analysis of ICT, MDA and FPT test coverage. All component models should be stored in an open architecture, non-vendor specific library format. This neutral format should be automatically generated using translation tools provided with software that will translate vendor specific model libraries into the neutral format.

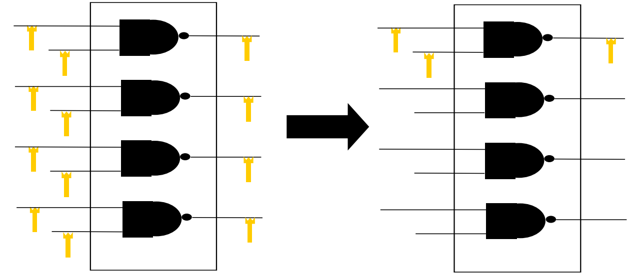


Figure 3: Probe reduction technique on a multi-unit analog or digital device - assumes automated inspection step is used for shorts and opens detection on each pin of the device.

The library device models provide pin function and device structure information that allows the software to make intelligent decisions regarding in-circuit test access requirements for multi-unit analog and digital devices. This would include, for example, identification of individual resistors within a resistor pack to provide single unit tests.

The software should also identify pure boundary scan nets and their required test access port (TAP) access for probe removal techniques.

Complementary And Overlapping Fault Coverage

Different factors constrain test strategies on boards that serve different marketplace requirements. Sometimes the constraining factor is "access" in which case the software can be used to deliver a complementary test approach between ICT and AXI for example. This complementary test approach could be executed in two ways, both should be supported by the software - the preferred approach depends on business requirements:

1. Maximum AXI complemented with simplified ICT. This strategy achieves maximum probe and test pad reduction because it assumes that shorts and opens will be tested on each and every pin at AXI, and furthermore that overlapping shorts/opens coverage on these same pins is not required at ICT. With this methodology, ICT is used only to verify that a functional part of the correct value has been placed at the location with the correct orientation. This can

be achieved by testing only one unit of a multi-unit analog or digital device as demonstrated by Figure 3 above. This is one example of a complementary test approach where the test methods are used in a manner to minimize their fault coverage overlap and achieve maximum probe reduction (3 probes vs. 12 in this example). DFT software can be used early in the design cycle to deliver a test plan that minimizes the requirement for test pads and fixture probe count. Thereby reducing fixture cost, complexity, weight, debug time and lead-time - a desirable strategy for boards with limited access and in manufacturing environments that struggle with fixture repeatability issues on high probe count boards.

2. Maximum ICT complemented with simplified AXI. On the other hand, other manufacturers may want to pursue strategies with maximum ICT on boards with limited access followed by selective AXI to fill the test coverage gaps at ICT due to loss of access. Since ICT is generally a much faster test method than AXI, manufacturers with very high volume requirements might prefer this technique to (1) above. The software could be used to prioritize access requirements for designers prior to the layout routing stage of PCB design in order to selectively place test pads where they add the most test coverage. AXI could be used to only provide coverage where ICT does not have coverage, thereby minimizing the AXI test time.

Other types of PCBAs like airbag or avionics boards that are destined for high reliability applications often require overlapping test coverage to minimize the possibility of defect escapes. Understanding that no test method is perfect, some OEMs prefer a high level of overlapping fault coverage to ensure all possible defect opportunities are sufficiently screened. Effective DFT software should enable users to pursue both complementary and overlapping test strategies and to identify the degree of fault coverage overlap in their test plan to meet the quality and reliability requirements of the end use environment (see Figure 4 below).

Test strategies more focused on complementary coverage will tend to deliver higher throughput and lower cost than overlapping test strategies that verify the same fault types at multiple stages. The optimum test strategy depends on the end use application and user requirements for test access, throughput, cost, and reliability. Effective DFT software can help manufacturers understand, quantify and analyze these factors in order to strike a balance that is appropriate for the particular PCBA and their manufacturing business objectives.

Figure 4: Fault Coverage Screen Capture from DFT Software - the software provides visibility to which defect types within are tested at each test stage. Complementary and overlapping fault coverage can be seen. Reporting is at a component-pin level. Engineers gain visibility on both what is tested and what is *not* tested.

Fault Spectrum

0 Matches, 0 Selected

☑ Part Number ☑ Electrical Type ☐ Physical Type Enable All Disable All

Ref Des	Part Number	Electrical Type	Circuit Object	Defect	Enabled	XStation 2D Transmission 2D	GR1 Analog	GR1 Digital
C6	4399-0027-00	CAP	Pin 2	Solder Quality	☑	Tested	Not Testable	Not Testable
C7	4399-0027-00	CAP	Component	Missing	☑	Tested	Tested	Not Testable
				Wrong	☑	Not Testable	Tested	Not Testable
				Skewed	☑	Tested	Not Testable	Not Testable
				Value	☑	Not Testable	Tested	Not Testable
			Pin 1	Solder Short	☑	Tested	Tested	Not Testable
				Solder Open	☑	Tested	Tested	Not Testable
				Solder Quality	☑	Tested	Not Testable	Not Testable
			Pin 2	Solder Short	☑	Tested	Tested	Not Testable
				Solder Open	☑	Tested	Tested	Not Testable
				Solder Quality	☑	Tested	Not Testable	Not Testable
C8	4399-3093-00	CAP	Component	Missing	☑	Tested	Tested	Not Testable
				Wrong	☑	Not Testable	Tested	Not Testable
				Skewed	☑	Tested	Not Testable	Not Testable
				Value	☑	Not Testable	Tested	Not Testable
			Pin 1	Solder Short	☑	Tested	Tested	Not Testable

Reason:

Help Apply UnDo Close Excel

Am

Gaps in Test Coverage

As discussed above, the software should use analog, digital and boundary scan model library information to accurately predict fault coverage for ICT, MDA and FPT on a component-pin level. Users gain visibility as to the level of complementary vs. overlapping test coverage provided by each machine in their distributed test plan. In addition, the software should provide insight into what defects are not tested at any given test stage and therefore identifies where the test plan is missing coverage (see Figure 4). It is arguably as important for a test engineer to understand where there isn't fault coverage in a test strategy as it is to understand where there is. By treating the fault spectrum and the coverage of each test stage as completely independent entities, the software provides objective and unbiased insight into the test coverage problem.

Warranty Costs, Product Reliability and Field Returns

When engineers have the ability to identify where they *do* and where they *do not* have test coverage and to what degree that coverage is overlapped at other test stages, they can evaluate whether their test plan meets the reliability requirements of the end use environment. Field return rates, warranty costs and customer goodwill costs are substantial liabilities for all manufacturers; hence delivered product quality level is a key performance metric of any test strategy. Effective DFT software enables organizations to minimize exposure to these factors and ensure a level of product reliability that meets business requirements. Significant savings can be achieved through reduced warranty and field return costs[1].

CASE STUDIES

Case Study Methodology

Three test strategies were applied to particular PCBAs with limited ICT access using DFT analysis software. The test coverage and other performance attributes of each test plan were measured on each board using the software's reporting capabilities. Although the software could report test coverage on many types of defects like value, orientation, skew and missing devices – only test coverage on shorts and opens is shown in order to simplify the analysis and demonstrate results.

Analog, Digital and Boundary Scan model libraries were available to the DFT software to intelligently determine test coverage and eliminate ICT probe access (test pads) in areas where other test stages had overlapping or redundant fault coverage.

Case Study Probe Reduction Methods

The following access removal methods were used for ICT when another test stage (AXI or AOI) provided fault coverage:

- Single element testing of multi-element analog and digital devices in cases where another test stage had opens and shorts coverage on other pins (as described in Figure 3, thereby removing access on n-1 elements).
- Access for TAP signals only on boundary scan devices to verify correct part and orientation (shorts and opens on other pins are tested at another test stage or via a pure boundary scan net).

The following types of access removal strategies were not applied, however further access reduction could be achieved by applying these techniques:

- Boundary Scan Virtual Pins – Using boundary scan cells as virtual drive and sense resources to test non-boundary scan devices, thereby removing required access on these nets.
- Remove nail on one side of series termination resistors – Where series resistors are used in nets connecting digital devices, remove the nail from one side of the resistor and drive / sense through the resistor using the remaining nail.
- Unused single-pin nets – These are nets whose only connection is to a single unused device pin.
- Minimum tests on non-multi-element, non-boundary scan devices to verify presence, function and orientation only. If shorts and opens are tested at another test stage, access can be removed on many of the device pins. This requires modification of the library device models before software modeling and test execution.

Case Study Test Strategies

Three test strategies were analyzed on each board:

1. ICT (only)

- Description: ICT is the only test method used. ICT utilizes maximum access to the board to the degree that is provided by the design.
- Strengths: The most common process test strategy used in the industry today. Test coverage is not good when access is limited.

2. Transmission[4] AXI & ICT

- Description: Transmission X-ray is used to test as many accessible joints as possible on this double-sided board. ICT provides complementary shorts and opens coverage on those pins not accessible by Transmission X-ray and provides coverage on other component defects like correct part and orientation.
- Strengths: Highest throughput, lowest cost, combined AXI/ICT test strategy since transmission X-ray generally operates at triple

the throughput of cross-section X-ray. Provides greatly improved test coverage for boards with limited ICT access without sacrificing line beat rate.

3. Cross-section[4] AXI & ICT

- Description: Cross-section X-ray is used to test as many accessible joints as possible (generally upwards of 99%). ICT provides complementary fault coverage on other defects like correct part and orientation but is not focused on opens and shorts testing since AXI provides this coverage.
- Strengths: Combined AXI/ICT test strategy for high complexity boards destined for high reliability applications with highly constrained ICT access. Provides highest possible coverage and minimizes potential for field returns.

Case Study Boards

Board 1

- Double-sided, high density, high complexity
- Low volume
- High reliability end use environment
- Board dimensions 16” x 16.5”
- 33,325 joints
- 3408 components
- 8044 nets/signals

Board 2

- Double-sided, high density, high complexity
- High Volume
- Computing end use environment
- Board dimensions 16” x 14.5”
- 20,630 joints
- 3250 components
- 5128 nets/signals

Case Study Results – Software Modeling

The following results were observed when the board data was modeled using DFT software. This modeling can be performed prior to the layout routing stage of PCB design so that ICT access can be provided where it is most required, to eliminate overlapping tests, reduce ICT probe count and improve production throughput.

Board Type	***B1***	***B1***	***B1***	***B2***	***B2***	***B2***
Test Strategy	***1***	***2***	***3***	***1***	***2***	***3***
Test Strategy Description	*ICT*	*Transmission AXI & ICT*	*X-Section AXI & ICT*	*ICT*	*Transmission AXI & ICT*	*X-Section AXI & ICT*
% solder joints tested at AXI	N/A	39	100	N/A	79	100
% nets tested at ICT	83	83	50	90	81	54
% solder joints with shorts coverage	94	100	100	96	100	100
% solder joints with opens coverage	41	82	100	46	89	100
AXI test time [min]	N/A	1.0	3.2	N/A	0.9	2.9
ICT test time [min]	1.1	1.1	0.8	0.6	0.6	0.4
ICT fixture cost	$31,000	$31,000	$20,000	$19,000	$17,000	$12,000

Case Study Results – “Real-life” Production Environment[5]

The following results were observed when Board 1 was put into production. The detection rate of each strategy was measured using a population of 252 defects that represent the natural fault spectrum at a specific EMS company.

Board Type	***B1***	***B1***	***B1***
Test Strategy	***1***	***2***	***3***
Test Strategy Description	*ICT*	*Transmission AXI & ICT*	*X-Section AXI & ICT*
% Real Defects Detected in Production Environment (252 total defects)	34%	76%	92%

Case Study Key Points

- The predicted coverage using the DFT software was close to the actual coverage achieved in a real production environment.
- The use of a combined AXI and ICT method (strategies 2 and 3) on boards with limited test access improves test coverage over an ICT only method (strategy 1).
- ICT access reduction and fixture cost reduction was greatest in test strategy 3 for both boards because AXI test coverage is also highest in test strategy 3.
- Although strategy 3 delivers maximum AXI test access and maximum combined fault coverage, note that AXI test time in strategy 3 is more than three times the test time of strategy 2.

- Although strategy 2 provides little access reduction over strategy 1, fault coverage is significantly improved over strategy 1 despite the fact that transmission AXI test access on board 1 and board 2 is 39% and 79% respectively.
- Strategy 2 is preferred for high volume products with cost sensitivity that require improved long term reliability.
- Strategy 3 is better suited to products that are lower volume, not as sensitive to manufacturing costs and that have a very high field failure cost.

CONCLUSIONS

Engineers have used past experience or subjective preference as a means for assigning test strategies to new products without analyzing the benefits and weaknesses of various different test approaches in a quantitative manner. Modern PCBAs in our cost and quality competitive environment require a more optimized strategy for each and every PCBA.

DFT software tools that enable testability analysis during board design allow test engineers to work concurrently with designers. They can predict the fault spectrum, plan test strategies, understand fault coverage and test access tradeoffs prior to the layout routing stage of PCB design. The benefits of using effective DFT software are: fewer design iterations, better test access, improved fault coverage, fewer snags, lower production test costs, improved time to market, improved shipped quality and lower field return costs.

Case study results demonstrate that coverage predicted by DFT software is realistic when compared to actual fault coverage achieved in production. Using DFT software during PCB design to model the fault coverage of different test strategies and make ICT access tradeoffs can significantly reduce cost and improve quality. Defect capture rates more than doubled when using alternate test strategies and production line beat rates varied significantly depending on the test strategy chosen. When DFT software enables these decisions early in the product life cycle, both OEMs and EMS providers can win by driving cost reductions through the entire product life cycle from NPI through manufacturing and warranty.

DEFINITION OF TERMS

Glossary

Distributed Test
A test strategy that leverages the strengths of various test machines (as measured by their fault coverage, access, test speed, diagnostic resolution or other attributes) in both complementary and overlapping manners to achieve a combined performance that optimal for the business requirements.

Fault Spectrum
The defect type possibilities and the locations where they may occur on a PCBA.

Fault Coverage
The effectiveness of a test stage at detecting a specific defect type on a location that is fully accessible.

GENCAM
IPC Standard 2541. This standard establishes requirements and other considerations for the interchange of information between electronic manufacturing software equipment and factory information systems. Information may consist of attribute and parametric data, product data, process recipes, equipment monitoring and control, resource utilization and material consumption. For more information, see www.gencam.org

Process Test
“Process Test” or “Structural Test” means all test and inspection operations prior to Functional Test. These test and inspection stages are generally focused on verifying correct assembly of the PCB (not functionality).

Test Access
The level of access that the test stage has to the PCBA. For example, ICT can have less than 100% access to the signals on the PCBA while transmission[4] AXI can have less than 100% access to the solder joints on a PCBA. The concept of test access is independent of "fault coverage".

Test Coverage
Test Coverage = "Fault Coverage" x "Test Access"

Testability Analysis
All available CAD and BOM information are used to determine ICT physical access. In addition, the fault coverage of other test stages like AXI, FPT or AOI are factored in to the test coverage model and tradeoffs are made as to which test stages should provide coverage on which parts and pins. Any lack of access is investigated and test pad requirements are determined based on the fault coverage of all test stages (not just ICT) and the model library information (BSCAN, analog, digital).

List Of Acronyms

AOI	Automated Optical Inspection
API	Automated Paste Inspection
AXI	Automated X-ray Inspection
BIST	Built in Self Test
BSCAN	Boundary Scan IEEE 11.49.1
CAD	Computer Aided Design
CEM	Contract Electronics Manufacturer

DFM	Design for Manufacturing
DFT	Design for Test
DFx	Design for Test & Manufacturing
EMS	Electronics Manufacturing Services
ESS	Environment Stress Screening
ICT	In-Circuit Test
FPT	Flying Probe Test
FT	Functional Test
HVI	Human Visual Inspection
MDA	Manufacturing Defect Analyser
MVI	Manual Visual Inspection (HVI)
NPI	New Product Introduction
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
QFP	Quad Flat Pack
RIP	Repair in Process
ROI	Return on Investment
SMT	Surface Mount Technology
TAP	Test Access Port [Boundary Scan]
WIP	Work in Process

ABOUT THE AUTHORS

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- Amit Verma is a Product Marketing Engineer at Teradyne Inc. in San Diego, CA since August 2000. Previously Mr. Verma was a Staff Engineer and Team-Leader at Celestica Inc. in Toronto, Ontario where he led automated inspection and complementary test strategies. Mr. Verma has over 7 years of hands-on user experience designing and implementing complementary and distributed test strategies for complex PCBAs. *amit.verma@teradyne.com*

[1] Teradyne Test Strategy Return on Investment Model, SMT Magazine Online, 09/01 "Effective Test Strategies for Modern PCBAs"
[2] See Glossary for definition of "Process Test" or "Structural Test"
[3] DFx = DFM & DFT. See Glossary
[4] AXI equipment is generally available in three forms:

- Transmission AXI – commonly referred to as "2D" X-ray
- Cross-section AXI – commonly referred to as "3D" X-ray
- Combo AXI – uses both "2D" and "3D" methods

Although the terms "2D" and "3D" are used pervasively in our industry, the authors believe these terms can be misleading and inaccurate in their description of transmission and cross-section X-ray technology. Because transmission X-ray captures information from the entire volume of the solder joint within the final gray scale image, transmission X-ray represents the solder joint volume in a more complete manner than cross-section x-ray which captures only a slice of the solder joint in the final gray scale image. Although in theory, multiple x-ray slices from a cross-section x-ray system can be accumulated to construct a volumetric model of the solder joint; today's cross-section AXI systems do not perform this operation and analyze only the two dimensional slices which lack the volumetric information from above and below the x-ray slice. Combo AXI equipment uses a combination of transmission and cross-section techniques concurrently during the inspection of a PCB. Combo systems automatically apply each technique where it is best suited and allow users the ability to prefer one technique over another if desired. This document will use the terms transmission, cross-section and combo x-ray and avoid the use of the terms "2D" and "3D" as these are inaccurate and misleading.
[5] Source : NEMI Test Strategy Project