

Best-Practice ICT Techniques and Benefits of Integrating GOPEL Electronics' SCANFLEX Boundary Scan System with Teradyne's TestStation



TERADYNE

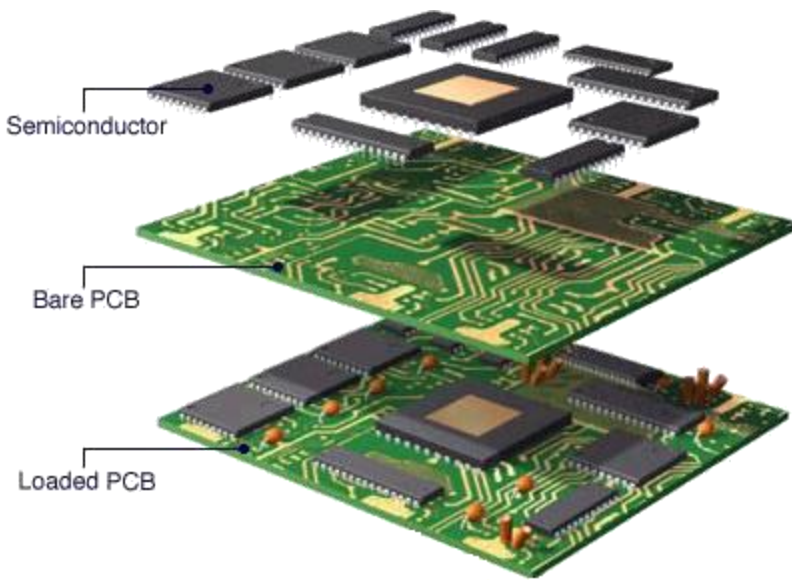
Assembly Test Division

- Basics of In-Circuit Test (ICT)
- Basics of JTAG/Boundary Scan (BScan)
- Benefits and challenges of integrating ICT and BScan
- Overview of SCANFLEX, integration in ICT
- SCANFLEX on TestStation / LH / LX / 228x
- SCANFLEX on TestStation SE / Spectrum
- Conclusions

Basics of In-Circuit Test

What is In-Circuit Testing (ICT) ?

- In-Circuit Test uses electrical test methods on printed circuit board assemblies
- ICT isolates components so each can be tested individually without influence of its surrounding parts



ICT Strengths

- Simple test generation
- Good fault coverage
- Fast throughput
- Excellent diagnostics

Test Coverage

- Full shorts test coverage
- Open device pins
- Analog component value and tolerance
- Digital component functionality
- Boundary scan and Built-In Self Test
- Full cell memory tests
- PLD programming



Test challenges for ICT

- Loss of access due to increasing board and device package densities
 - Need for reduced access tests and cluster tests
 - In-system programming of FPGAs, CPLDs, and Flash
 - Support of advanced test methods and standards
 - IEEE 1149.6, 1532, STAPL
- ➔ Alternate techniques needed to address ICT gaps

Tackling those challenges

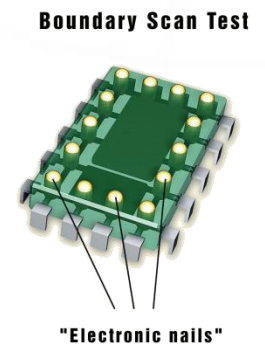
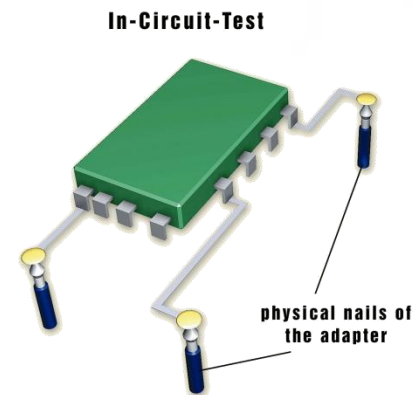
- Employment of supplemental test/inspection techniques (such as Boundary Scan, AOI, and AXI)
- ICT can be enhanced with added value techniques like Boundary Scan and FLASH / PLD programming
- Implementation of a distributed test strategy

Basics of JTAG/Boundary Scan



Benefits of Boundary Scan:

- Low ATE and test development costs
- Electrical test access to hidden pins (e.g. BGA)
- Improving time-to-market
- Provides easy access to BIST resources
- Provides access for In-System Configuration

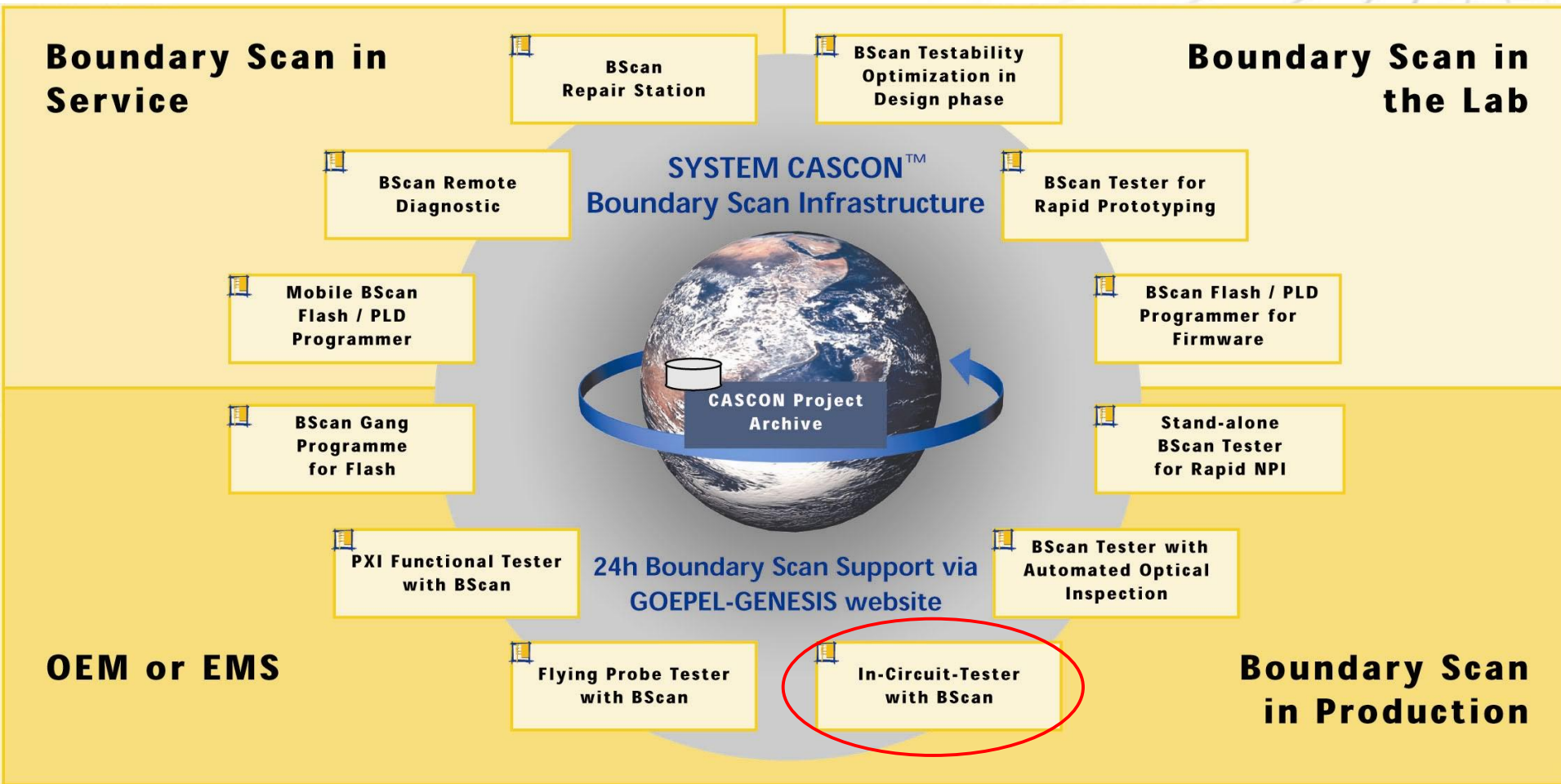


Boundary Scan (JTAG)

- Find structural faults (stuck-at, open, short) on the PCB
- Full access not required in all cases
- No “back-driving”
- Test execution is a matter of seconds
- Input: CAD data and BSDL files;
automated test generation (ATPG)
- Use throughout whole product life cycle (PLC)
- Requires UUT to be powered up for test
- In-System Configuration → additional cost savings



Boundary Scan throughout PLC



Benefits and challenges of integrating ICT and BScan

Integration of Boundary Scan in ICT supports:

- Improving overall fault coverage and diagnostics
- Sharing of test resources
- Simpler, less expensive test fixtures
- Reduced handling (one location for ICT and BScan)
- ICT resources available for BScan test for isolation
- Unlimited In-System Programming (PLD, FLASH) via Boundary Scan
- Reuse of test programs throughout product life cycle

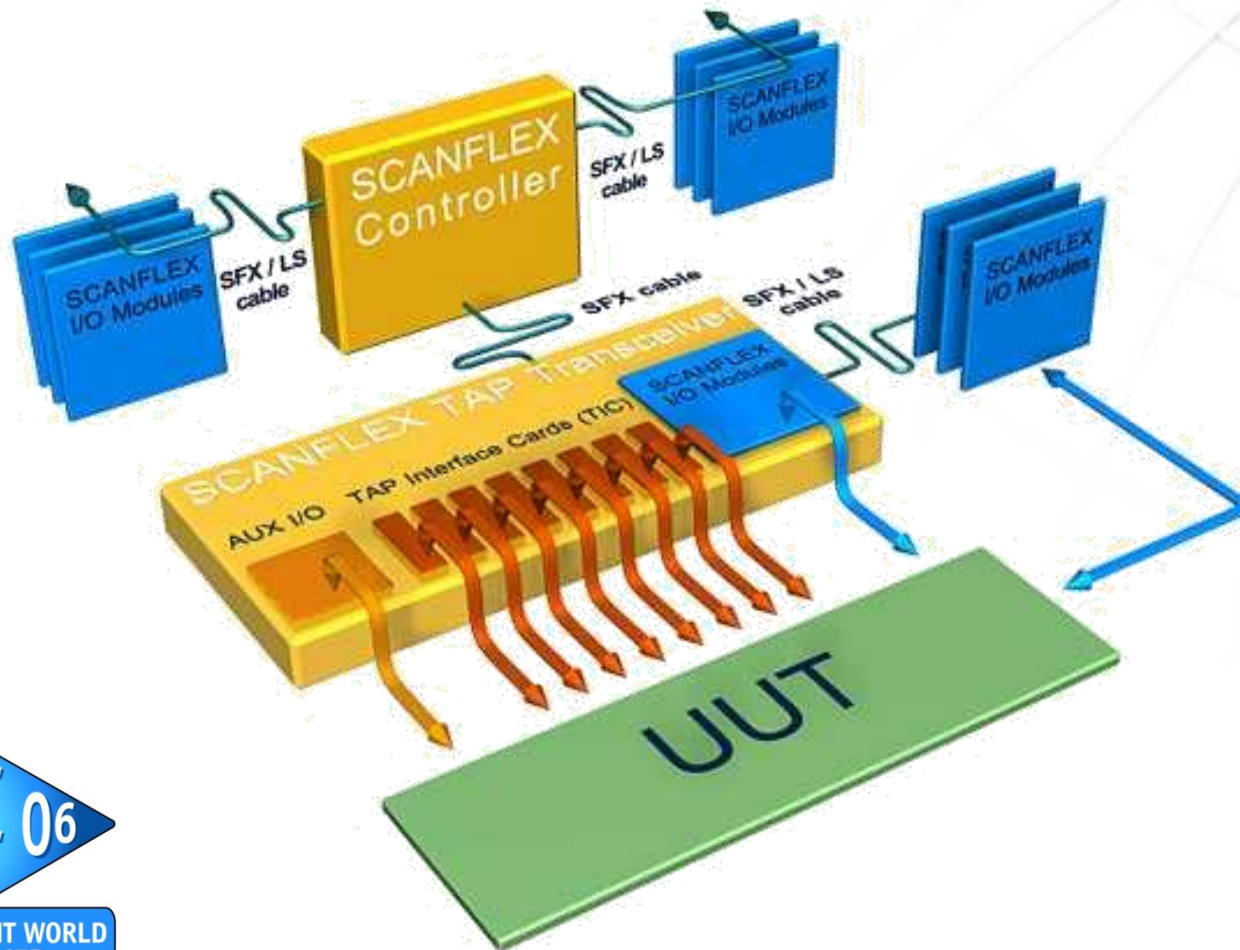
Challenges of integration

Integration of BScan in ICT also poses challenges:

- High-speed signals on IEEE 1149.1 test bus
- Ground Bounce
- Signal noise
- Software handshake for test execution
- Shared test resource control

⇒ A well designed integration overcomes these challenges

Overview of SCANFLEX and Integration in ICT



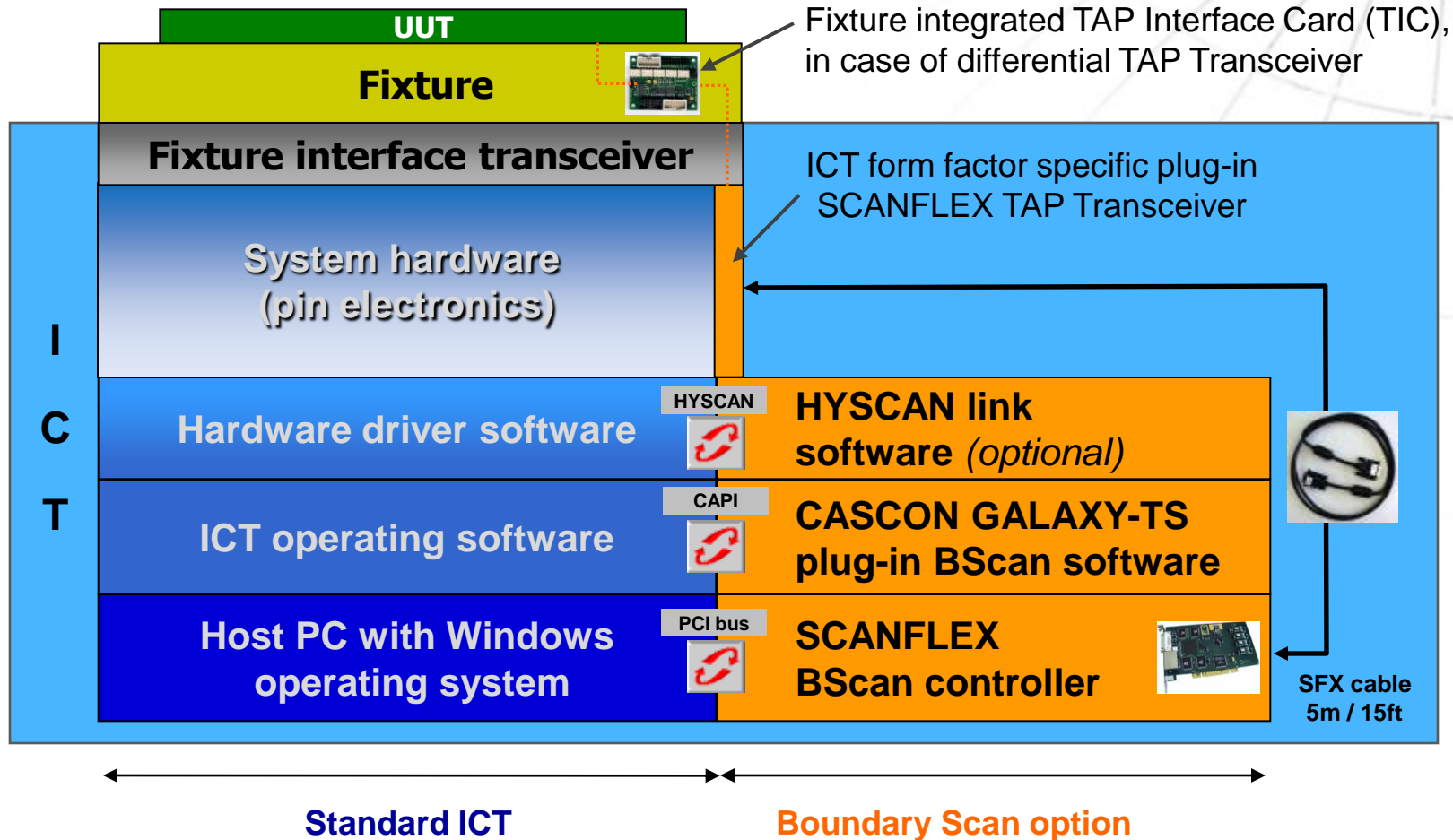
TEST & MEASUREMENT WORLD
AWARD WINNER

- Superior modularity, flexibility, performance
- SFX Controller, SFX TAP-Transceiver, SFX I/O-Modules
- Up to 80MHz TCK,
Up to 8 independent, programmable TAP,
32bit PIO, 2 analog I/O, trigger signals
- Special H/W features to improve throughput
- Special TAP Transceivers for ICT integration:
 - Differential (fixture modules) or single-ended TAP signal transmission
 - Relays-coupled TAP and PIO signals

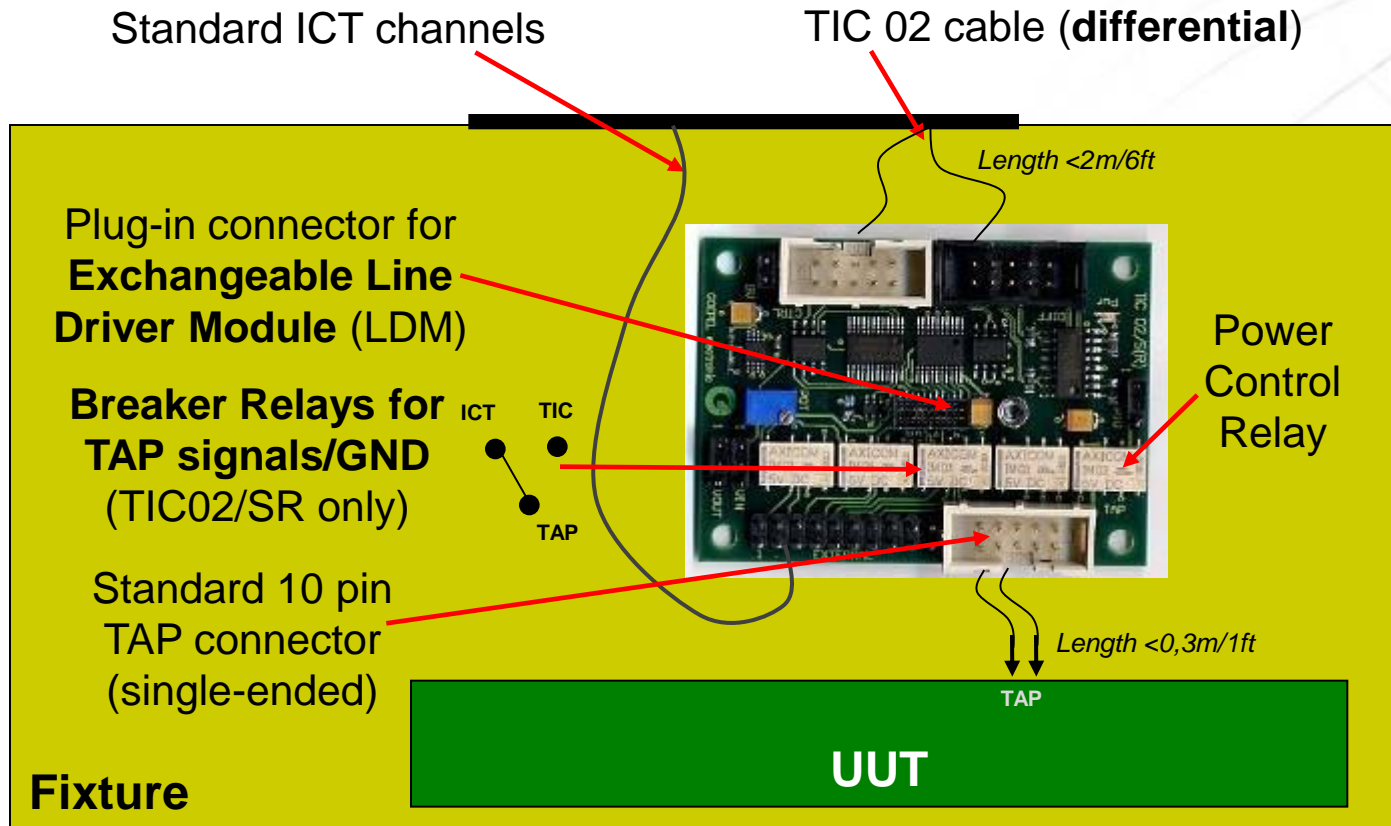
Special TAP Transceivers for ICT integration:

- **SFX/TAP4-xxxx/FXT** with 4 TAP's
(differential TAP signal transmission between TAP Transceiver and fixture mounted TIC modules)
- **SFX/TAP4-xxxx/PIC** with 4 TAP's
(single-ended TAP signal transmission between TAP Transceiver and test points)
- **SFX/TAP8-xxxx/PIC** with 8 TAP's
(single-ended TAP signal transmission between TAP Transceiver and test points)

SCANFLEX in ICT (differential TAP)



SCANFLEX in ICT (differential TAP)



Default TIC02 with In-Line Resistors on LDM



Available LDM for

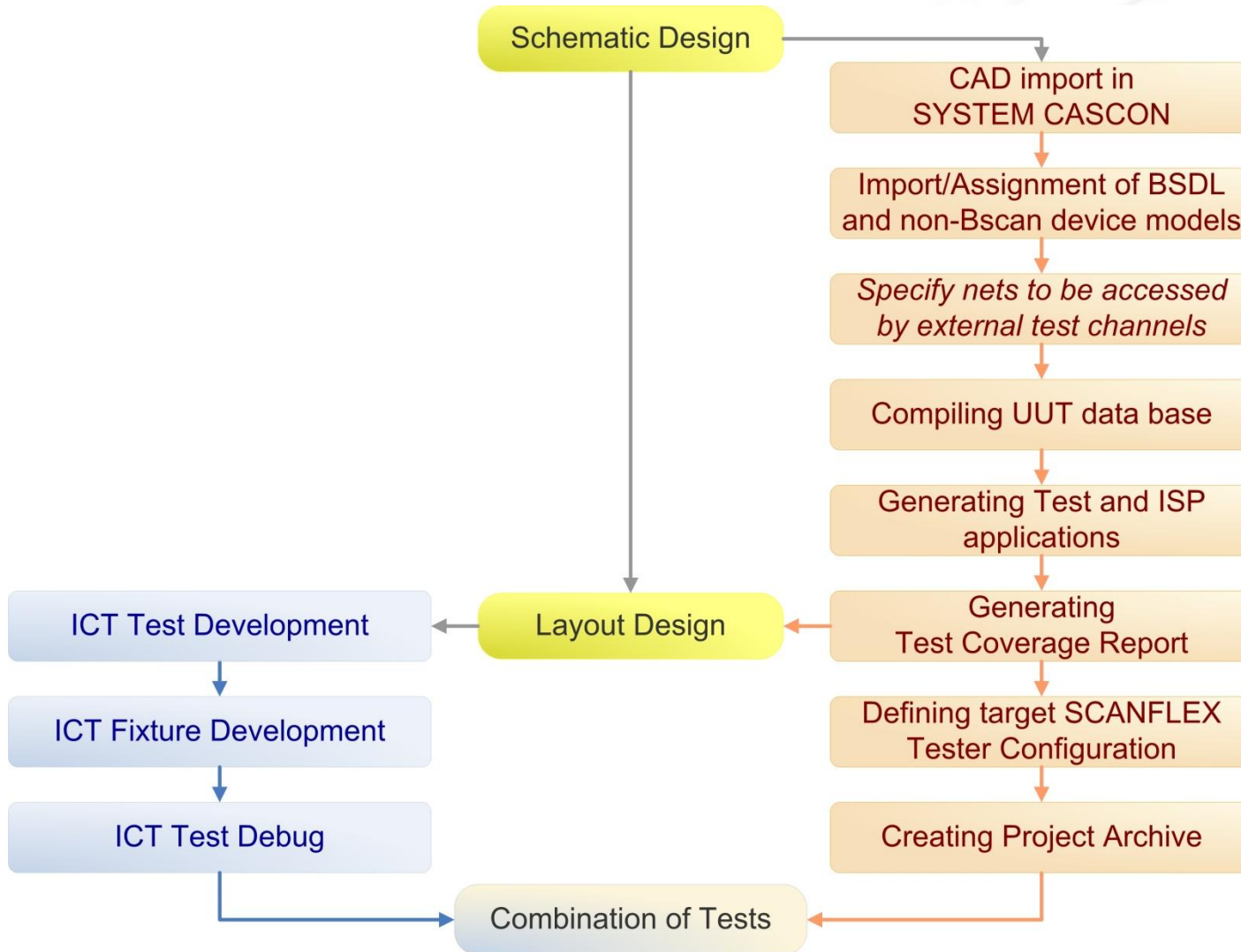
- GTL Interface
- high current
- and more

- TIC02 offers additional features controllable by software
- TIC02 enables up to 2m@80MHz high speed JTAG signal transmission
- Exchangeable Line Driver Module (LDM) enables easy interface customization

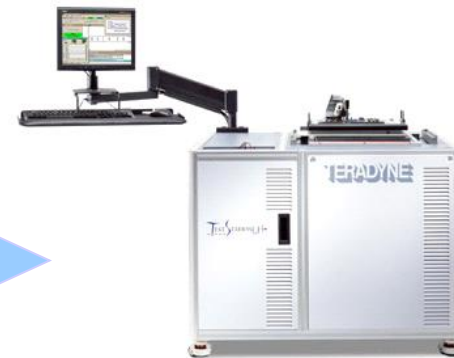
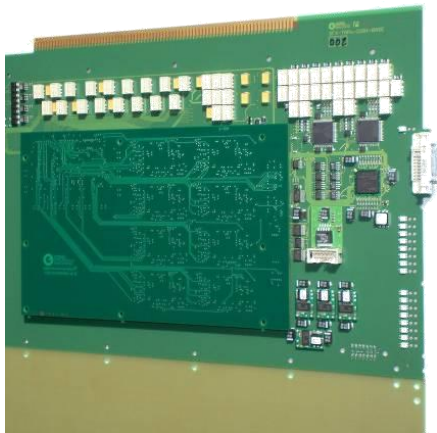
- PCI (or other hardware platform) based SCANFLEX Controller;
- Special TAP Transceivers for Teradyne ICT with programmable TAP interface parameters and relay coupled TAP and PIO resources;
- Reuse of stand-alone BScan Test and ISP (FLASH, PLD/FPGA) routines;
- Optional reuse of extended BScan Test routines utilizing ICT tester channels controlled via HYSCAN (a SYSTEM CASCON feature);
- Integrated software control via CASCON API;



Example Test Development Flow

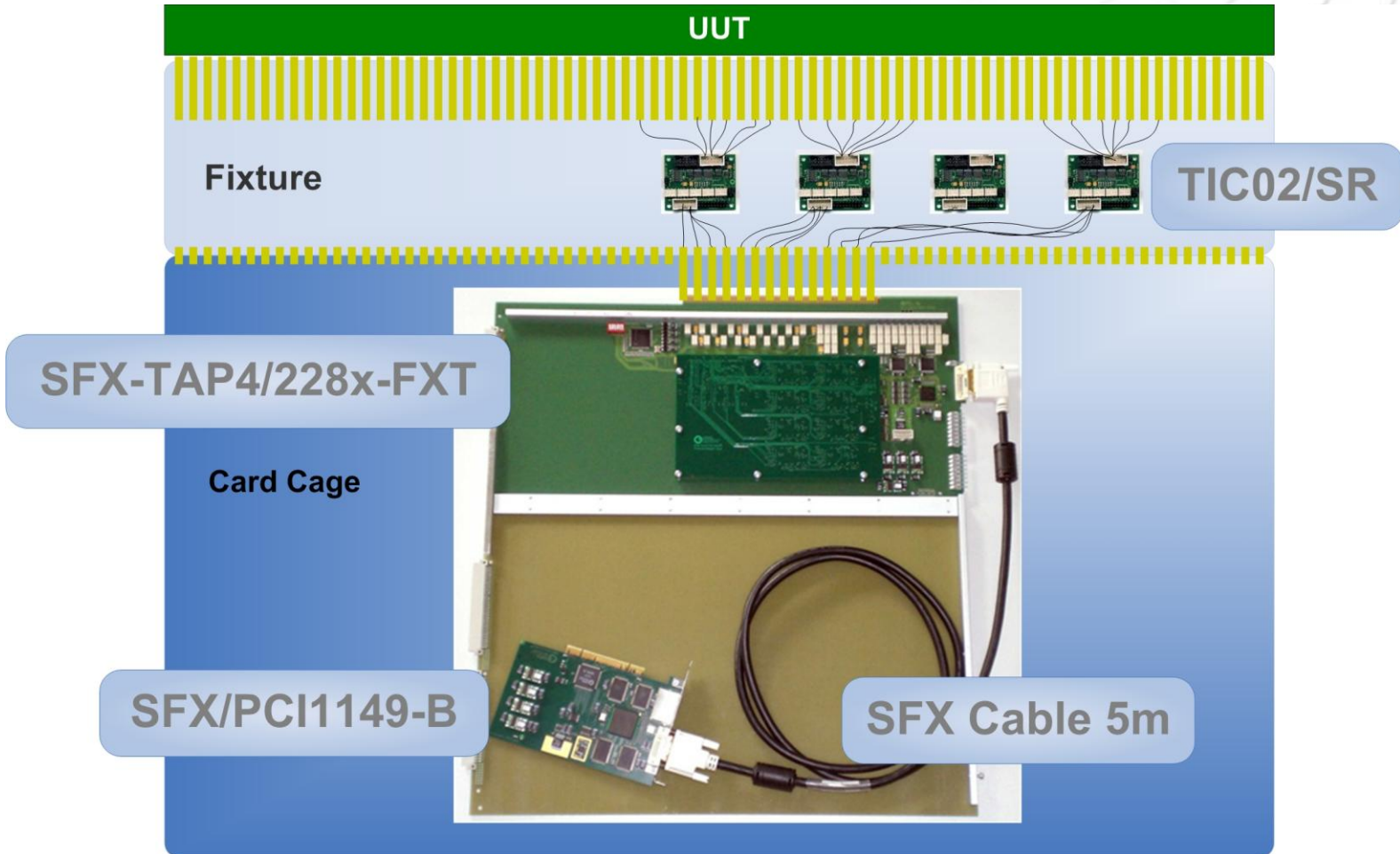


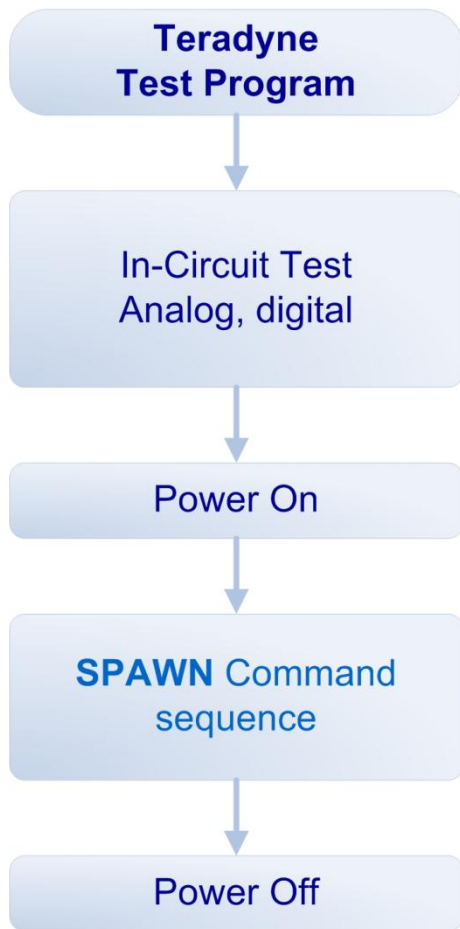
SCANFLEX on TestStation LH / LX / 228x



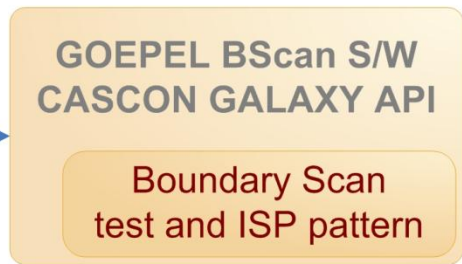
Integration overview – Hardware

(here for differential TAP Transceiver configuration)





SPAWN commands call CASCON API functions via special Communication Link Software



Communication link software

Communication Link Software commands:

<code>casconcmd.exe -s</code>	Initialize CASCON API
<code>casconcmd.exe -u</code>	UUT_NAME Select CASCON UUT
<code>casconcmd.exe -t</code>	TEST_NAME Select CASCON Test
<code>casconcmd.exe -b</code>	BATCH_NAME Select CASCON Batch
<code>casconcmd.exe -xt</code>	Execute Test
<code>casconcmd.exe -xb</code>	Execute Batch
<code>casconcmd.exe -c</code>	Close CASCON API

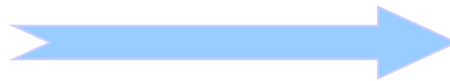
Commands in TPG:

```
CALL SPAWN (TMP='CASCONCMD.EXE -XT');
```

Commands in DOS batch file:

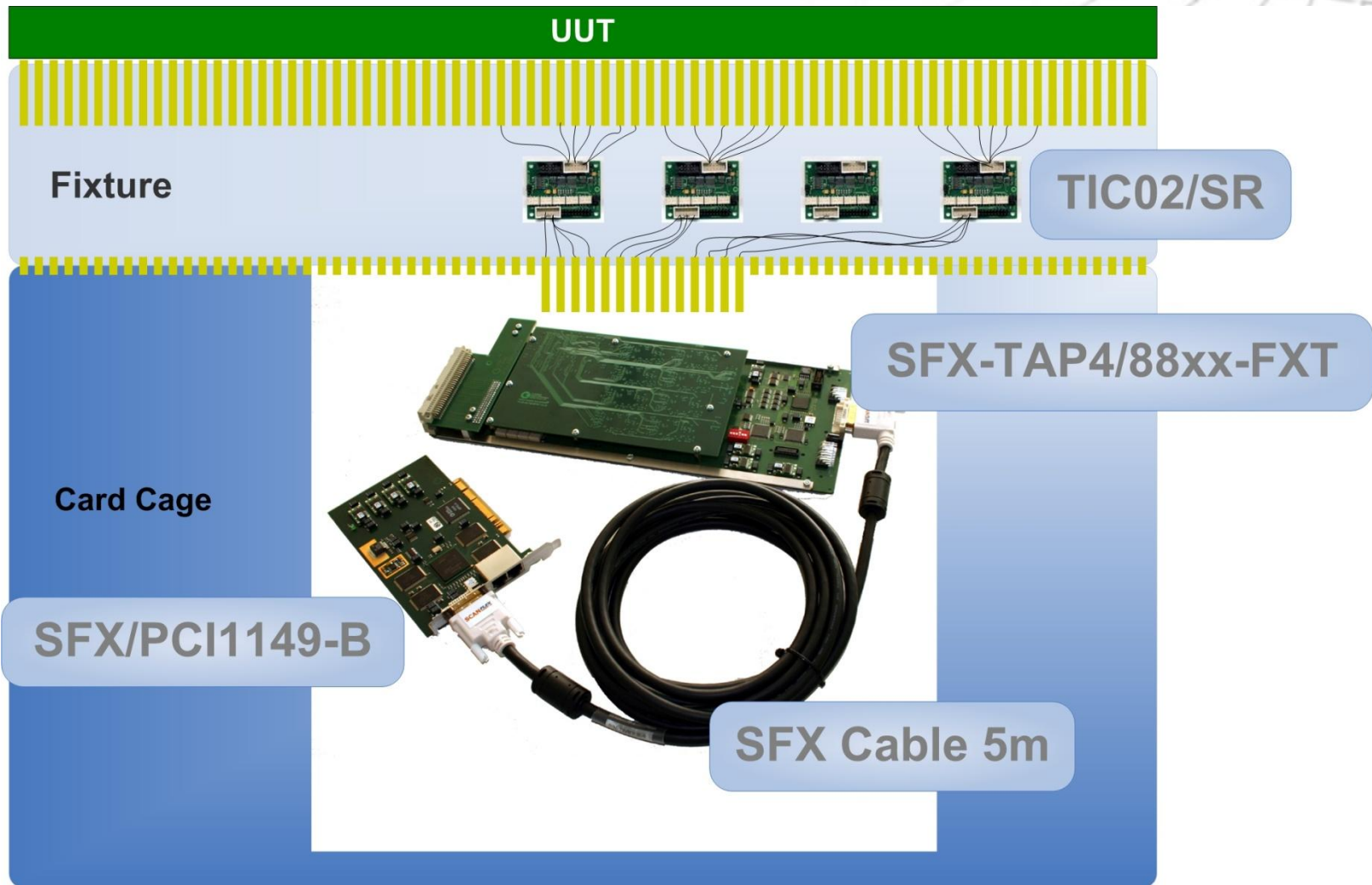
```
CALL SPAWN (TMP='GOPEL.BAT');
```

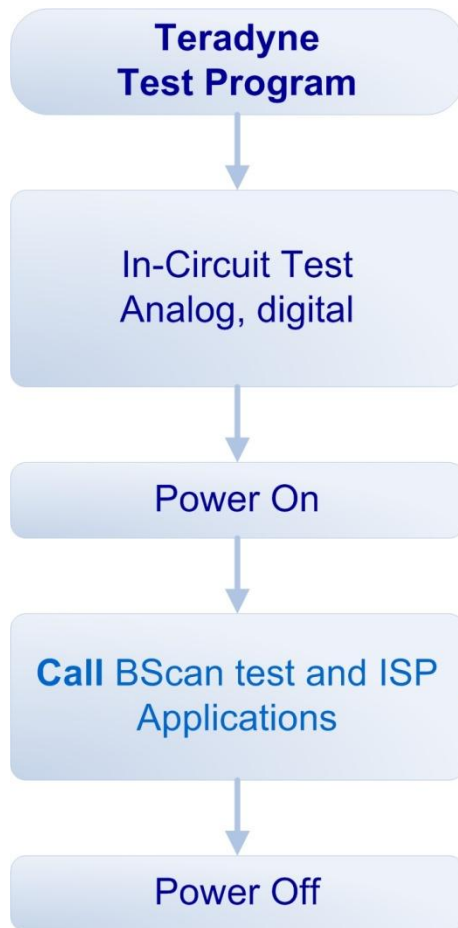
SCANFLEX on TestStation SE / Spectrum



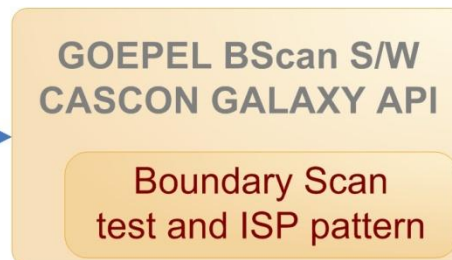
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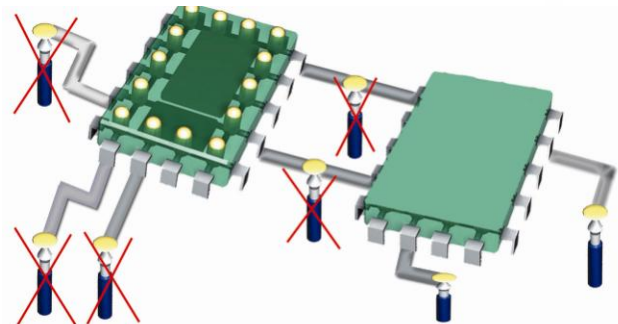


- CASCON API calls directly from TestStation SE software
- Control of SFX resources by CASCON
- Control of ICT pin electronic by TestStation



Conclusion

- Integration of Boundary Scan and ICT can increase fault coverage and improve diagnostics while lowering cost of test
- SCANFLEX offers unique features for ATE integration
- Collaboration of Teradyne and Goepel to offer best possible integration
- Proven at customer production sites



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