

Applying Virtual Test Principles to Digital Test Program Development

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Abstract - Simulation model development and test program integration can account for over half the effort spent on digital TPS development. Digital test development in a Virtual Test environment can result in substantial TPS cost reductions through a combination of VHDL device model reuse and ATE environment simulation. Technology developed under the VTest contract sponsored by the U.S. Air Force Wright Laboratory Manufacturing Technology Directorate enables fault simulation of devices supported by VITAL libraries, thereby extending the use of VHDL into test program generation. Simulation driven VTest methodologies enable development of digital test programs completely off-line and with the ability to target virtually any digital ATE.

I. INTRODUCTION

The objective of Virtual Test is to achieve significant reductions in the cost of initial test program development and in test program rehost effort. These reductions in cost and effort can be attributed to the use of simulation that enables virtual development and integration of test programs on ATE, and the reuse information, generated in the design process, for test development and execution. To define where these reductions can occur, we need to examine the digital test generation process and focus on improving those parts of the process where the greatest amount of time and effort is expended.

The test development process can be viewed as being composed of the following steps:

- Test requirements definition
- Determining the test limits
- Writing the test program
- Diagnostics and test program integration
- Documentation and program maintenance

Studies that Teradyne has conducted on its own user base have shown that the bulk of the effort (50%) is spent in the diagnostic development and test program integration stages of the process. A similar study by the Institute for Defense Analysis (IDA) arrived at essentially the same conclusion. (See Figure 1.)

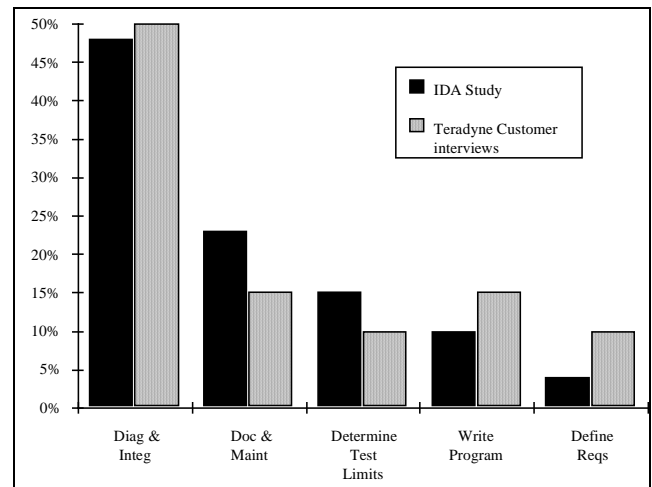


Figure 1. Teradyne and Institute for Defense Analysis studies confirm that most of the time spent in TPS development occurs during diagnostic development and test program debug.

The main reason for the large amount of time spent in diagnostics and integration is that after program code is written, it is compiled and checked out on the ATE. When errors in the code are detected, the program is rewritten or tweaked, then reverified on the ATE. Several iterations can occur before the code is completely verified. This is a highly inefficient use of development time and ATE resources. Simulation offers a powerful alternative and can be used on 75% of the test generation process described above. This is true for both analog and digital circuitry, though digital simulation technology is much further along in its ability to generate high-resolution diagnostic data. And while both analog and digital simulation can prove to be advantageous in test program development, the remainder of this discussion will focus on digital simulation.

II. SIMULATION AND MODEL REUSE AS THE VALUE BASIS FOR VIRTUAL TEST

The use of simulation for digital test program development offers several advantages:

- Automatically generates good circuit response to a set of stimulus vectors. This is the basis for a Go/No-Go test.
- Provides a prediction of worse case timing behavior of the UUT (Unit Under Test) to the stimulus set.
- Provides a means for predicting the effects of the test equipment (ATE channel cards, test fixture) on the UUT prior to actual test integration.
- Automatically predicts the quality of the test in terms of fault coverage and diagnostic resolution
- Automatically generates diagnostic data - guided probe and fault dictionary databases.
- Provides a means for accurately placing response capture windows on test equipment measurement ports - I/O pins and probe

With all its benefits, the value of digital simulation for test generation will only be as good as the device models used in the simulation. While this may be stating the obvious, this precludes the use of most simulation models that are targeted for design simulation.

For design simulation, the functionality described by a model must be able to be modified quickly, and support high levels of abstraction. They ordinarily don't support worst-case timing and fault simulation. In test simulation models, on the other hand, functionality is fixed, the level of abstraction is low, and worst-case timing and fault simulation are important simulation attributes that must be supported.

For these reasons, test program development requires a separate simulation model library that contains information germane to simulation for test. Unfortunately, model development for test simulation can account for up to 40% the effort spent on functional test program development. At this level of investment, the benefits that simulation bring to Virtual Test are hard to appreciate. It is here in the area of simulation model development for test where Teradyne as a VTest team member has focused its efforts. The result has been the introduction of the LASAR-VT option, the first stage of an initiative to advance the usage of VHDL model descriptions in simulation for test.

VHDL, in particular the subset defined in the VITAL standard, plays a key role in applying Virtual Test principals to digital test development. Herein lies the best conduit for reuse of design model descriptions in test simulations. VHDL circuit descriptions that can be defined in VITAL primitives offer the ability to verify design implementation through worse-case timing analysis and to perform fault simulations that provide

the raw data for high fault coverage, diagnostic test programs. (See Figure 2). Best of all, VITAL libraries are a by product of the design process, thereby providing models for test simulation derived from the same synthesizable VHDL descriptions used in design

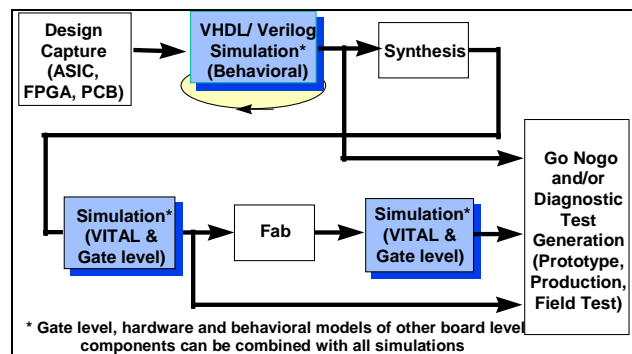


Figure 2. Through the use of models described in VITAL and Register Transfer level VHDL, virtual test simulations providing detailed timing and fault analysis can be supported

The process of ASIC and FPGA design typically involves the use of VHDL and Verilog design tools. High-level behavioral descriptions of a circuit ultimately get refined to a state where they can be imported by a design synthesis tool, and converted into a form of interconnected macrocells that a foundry can physically implement in silicon. For example, if the target foundry is Actel, the synthesis tool would output the synthesized design in a format that Actel reads. Actel supports VITAL and can provide to its customers a library of all macrocells elements in the design in VITAL. All this without the circuit designer having to do anything extra or different from what would ordinarily be done to develop the circuit. The netlist used to define how the macrocells are interconnected is also a by-product of synthesis.

By using a test simulator, such as LASAR, that supports VITAL, the full board design, as well as the ASICs and FPGAs making up the board design, can be verified under worst-case timing conditions and fault simulated to determine fault coverage. The results of this simulation can then be used to quickly produce Go/No-Go and diagnostic test programs for prototype board testing. This same design and test database can be reused to retarget the test program for production test. All that's needed is to simply update the tester environment model for the new target test system, and resimulate to produce the test program database.

VITAL libraries are available from all major ASIC and FPGA suppliers for device families introduced after 1995. Users can request the library of macrocells for

a specific design, or the entire macrocell library for a family. If several devices from the same family are going to be designed and simulated, the user is better off obtaining the entire library of macrocells for the family. This way, only the netlist for subsequent devices is required to import the design into the test simulator.

III. TEST PROGRAMS ARE A PRODUCT OF THEIR ENVIRONMENT

Test program integration is another cost driver that can be effectively addressed in a Virtual Test environment. Problems that plague test integration include:

- Intermittent signal timing problems caused by the delays and skews introduced by the UUT interface and the ATE drive/detect channels.
- Signal or test pattern incompatibilities between the test generation tool and the target tester.

Signal-timing problems caused by misplacement of edges in a pattern can be very difficult to diagnose because it is only one of many potential problems that can exist when a test program is undergoing check out on the hardware for the first time. Is the failure due to the program, the UUT, the test fixture, the ATE? Hours can be spent with a variety of external test equipment - scopes, probes, logic analyzers - trying to diagnose the failure. A virtual test simulation that includes a model of the test environment can eliminate tester channel skew, fixture delays and tester channel drive problems from the list of potential hardware debug challenges.

To compound the issue, signal-timing problems can be very subtle, and frequently don't manifest themselves until after a test program is released. The reason is that during development, the test program code is only verified against a small sample of UUT's, whose range of variable signal delays is narrow enough to allow all of them to pass the program. But what about the board that is fault free, but fails the test because of an intermittent response, or because of signal timing hazards induced by the additional skews and delays introduced by the test environment? Hours, even days, will be spent debugging this problem, and in the end, will force an ECO to the test program, adding to the cost of test development. In addition, simulation of the UUT alone will not help. As Figure 3 illustrates, simulation of the UUT without taking into effect the test environment only confirms the response of the UUT as an isolated unit. Responses predicted during this type of simulation will not necessarily match those observed on the tester.

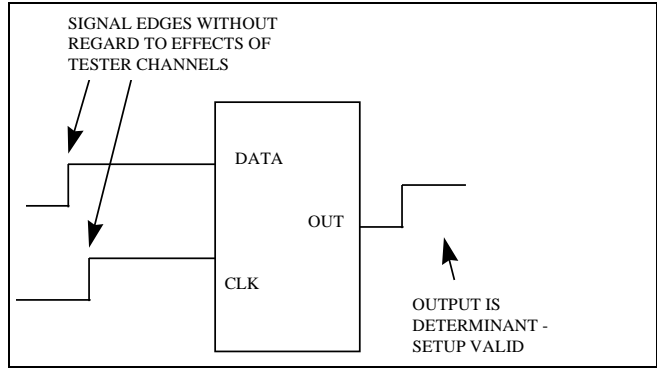


Figure 3. Simulations that do not model the test environment can mask potential UUT performance problems.

In a Virtual Test environment, characteristics of the ATE's digital test channels, and the UUT interface hardware can be modeled and included in the test simulation. Problems that would ordinarily be detected on the ATE during test integration can now be detected during simulation, and corrective actions can be initiated quickly and easily.

Furthermore, the test environment characteristics can be changed quickly and resimulated to generate test data for another target ATE. These ATE characteristics can be stored in a TeRM database and reused for the next test that is targeted to that ATE and interface.

When the same simulation is run with the test environment model added (illustrated in Figure 4), potential timing hazards can be easily detected and corrected in a virtual test simulation at a time in the product development process where changes in the pattern set are easily made and verified.

Another benefit of test environment modeling and simulation is that different target environments can be verified against the tests developed for a specific UUT. This is an enormous benefit in the sense that

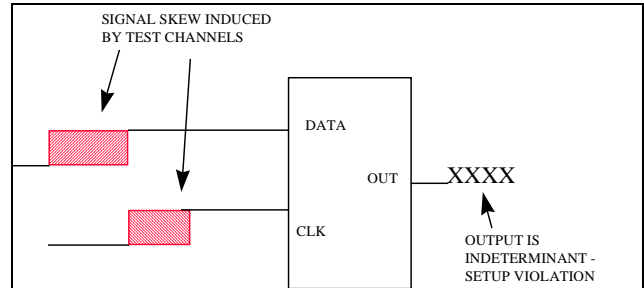


Figure 4. A simulation that includes a model of the test environment provides the insight into test program debug problems that can take significant time and effort to debug on the ATE.

two test programs can be generated from the same test development database - the second test program carries essentially no development cost. To verify

digital tests against other target environments involves resimulating the test using the models for the other environments.

These types of problems can lead to days of debug time on the ATE and significant rework of test programs resulting in slipped schedules, missed opportunities and cost overruns.

IV. EXTENDING THE REACH OF DIGITAL VIRTUAL TEST

VITAL model usage in a digital virtual test simulator such as LASAR is the beginning of a series of efforts by Teradyne aimed at improving model reuse from design. The next phase of the VTest project is focusing on the use of pre-synthesis VHDL models and post-synthesis Verilog models for fault simulation and dynamic timing analysis. To further extend the reuse of traditional design modeling methodologies, work is in process to support fault simulation and worst-case timing for test simulations using Synopsys SMART Models.

To understand the value of accurate simulation at the pre-synthesis stage, one needs only to refer to the

“times ten rule” for detecting faults in physical product. Detecting a fault at functional test costs ten times more than detecting it at in-circuit test. Detecting a fault at system test is ten times more costly than detecting it at functional test. This same principal can be applied to the design process. Detecting a design error after layout is ten times more costly than detecting it right after synthesis, and so on.

In today's competitive business environment, time to market is critical. Anything that can reduce the time it takes to get a product working, producible, and testable in production volumes is a valuable addition to the product development process. Equally important is the need to reduce the risk of a critical failure in a product. Accurate timing simulation can detect critical design flaws that functional verification alone can easily miss. Advances in digital simulation technology being developed under the VTest project can help provide the competitive edge, and reduce the time to achieve it.

V. CONCLUSIONS

The VTest project has been the catalyst for enabling the development of tools and methodologies for a commercially viable digital Virtual Test solution which reduces test program development time through design model reuse and test environment simulation. With the introduction of Teradyne's LASAR-VT option, VITAL compliant models can be used in a full board fault and worst-case timing simulation to provide tester independent digital test program source data. VITAL models are by-products of the product development process and can be used without modification for design verification and test simulations, thereby saving weeks of simulation model development effort. By including a target test environment description, and simulating it in LASAR, weeks of test program integration and debug time can be shaved off the task of developing test program sets.