

# Replacing Legacy Digital Test Instrumentation

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## Abstract

The purpose of this paper is to examine the complexity for replacing high performance digital instruments in aging test systems and the factors that impact the transition. Those factors include software integration and changes in basic functionality and in parametric performance. To demonstrate the transition, three instrument replacements are described where the process is broken down by the requirements, efforts, obstacles and countermeasures involved in engineering a solution.

Keywords: digital, instrumentation, legacy, replacement

## 1 Introduction

The military is continually extending the expected life for electronic systems, therefore demanding the test support equipment to match the extended life cycle requirements. Unfortunately, these systems and subsystems are used by the military and commercial industries and due to the nature of the rapid development in the commercial electronics industry, many parts and subsystems are becoming obsolete. This has an impact for both the instrument manufacturers as well as test station designers. Often the result is testers require modernization to effectively support their respective systems. There are two methods to handle this problem. The first involves re-hosting the test program sets (TPS) to a new tester, one that can support the program life. The second method is to give the existing system a face-lift, hence replacing obsolete components with current components that can be supported. Although a new test system may seem attractive, the desire is to preserve the fielded TPSs investment due to cost benefits. A mantra to consider: Newer is not always better. Ultimately, instrumentation needs to be upgraded while preserving as much of the TPS investment as possible. When evaluating the requirements to replace an existing instrument with a newer design, there are three major areas of concern: software, feature set, and parametric values.

Software is an important factor when considering how best to maintain isolation between the TPS and the instrument. In many legacy systems the ATLAS language provides this isolation by expressing the test program in signal-based syntax. Recently an industry initiative called the Interchangeable Virtual Instrumentation Foundation (IVI) was formed to provide software interchangeability in a non-ATLAS environment. In general,

these approaches work well with simple analog instrumentation where there is a high degree of functional overlap and the parameters are well defined. For complex instruments, including digital stimulus and response, quite often ATLAS programs resort to non-ATLAS syntax or system specific extensions of the ATLAS language to enable testing of digital electronics.

The feature set for the existing and replacement instruments is a concern when replacing digital instrumentation. Simple digital stimulus and response, as defined in the first revision of the IVI digital class specification, or in the 1985 or 1989 versions of ATLAS, cover only rudimentary functionality. Digital test equipment complexity and comparison between instruments become harder when the timing, synchronization and pattern sequences are taken into account. These features are often based on a specific hardware implementation that varies greatly between instruments. If these features differ, then a decision needs to be made to either modify the architecture of the replacement system to emulate the existing system, or modify the TPSs that exercise the features.

Even if the replacement system matches the software and feature sets identically, there can still be problems in matching the parametric values of the two systems. In many cases, the new system will have a different circuit interfacing to the unit under test (UUT). This could be the result of obsolescence or improvements to the technology. This can give rise to both known and unknown problems. In some cases the known areas may not be match able, such as over voltage protection that may cause test programs to fail, or in extreme cases may damage the tester or the UUT. In other instances test programs may depend on inherent characteristics of the tester that may be unspecified. These characteristics like leakage current or high impedance value may not be match able. In these extreme cases, the only option is to modify the TPS to depend only on a specified performance.

## **2 Background**

Several customers have approached Teradyne with a need for new digital test capabilities. In some cases, there was a desire to move from a proprietary system to a COTS package as part of a modernization effort. In other cases, like the CASS program, a new design and new technology offered cost savings in logistics, maintenance, and extend life supportability. Then there are customers who could no longer build the existing capability, yet needed to service their new customers. The requirements for each of these situations gave rise to a different solution.

The notion of compatibility is easy to understand when discussing the evolution of a product. The design of the newer product is often based on its predecessor. In the case of the IFTE EOTF digital upgrade, a design by Northrop Grumman is being replaced by a design from Teradyne. While every effort has been made from the engineering perspective to ensure the replacement capability is able to perform all of the functions that the original system provided, there may be some instances where improved performance may not provide compatibility between systems, or where a test program used a parameter that was not specified (explicitly or implicitly). These cases are

difficult to identify. Teradyne and Northrop Grumman have worked together in an attempt to identify all of these issues for evaluation.

This paper will look at one of each type of these replacements, the transition from the IFTE BSTF to the IFTE EOTF system, the CASS Block 1 to Block 2 or VECP system, and a customer updating as system for the F-16 program. These are three example of digital instrument replacement that had differing levels of requirements that caused three different integration schemes.

### **3 Discussion**

#### **3.1 CASS Digital Subsystem Replacement**

CASS was originally fielded with the Teradyne M895 Digital Test Unit (DTU). Over 250 stations were fielded with a complex digital subsystem. Hundreds of TPSs were fielded with the M895 DTU. In 1994 Lockheed Martin and Teradyne proposed that the current DTU be replaced with a new version, including replacing the aging DEC VAX CPU with a DEC Alpha CPU. The reason for the replacement was a savings in the procurement and logistics costs. The new revision DTU was designed to have fewer replaceable components, and to use modern ASIC technology. However, the number of fielded TPSs required that the existing TPSs worked without modification on the new design. Furthermore, because this change was introduced after so many stations were fielded and an equivalent number were to be fielded with the new version, there was an additional requirement, that the TPSs developed on the new design would work on the old. This strict requirement applied to both software and hardware. This commitment to interchangeability was only possible because the hardware and software were provided by the same company along with complete design information.

##### **3.1.1 Hardware Replacement**

The M900 was designed to be the next generation digital test for Teradyne. The architecture was based on previous generations of L-Series testers. The intent of the engineering program was to provide a smaller, higher performance version of the M895 and L320 Series testers in an industry standard form factor. The design used state of the art custom digital and bipolar Asics to achieve greater density with improved performance. While the M900 architecture was identical to the M895 being replaced in CASS, the implementation varied. The overriding principle in the design stage was to provide 100% compatibility from the M895 to the M900. In addition to forward and backward TPS transportability, other key design goals included a 20% cost reduction, higher performance (50 MHz data rate), a 50% reduction in size, and higher reliability (>4,000 hours MTBF). As the manufacturer of the M895, Teradyne was in possession of all of the specifications and original hardware and software design information. Even with all of the data available, performance still varied in some areas.

**Table 1.** M895 vs. M900 Specifications [1]

<b>Feature</b>	<b>M895 DTU</b>	<b>M900 DTU</b>
Data Rate	20 MHz, 40 MHz Interleaved	50 MHz
Pattern RAM	16K x 5/Channel	64K x 5/Channel
Driver Accuracy	<u>+ 5nS</u>	<u>+3 nS</u>
Detector Accuracy	<u>+ 5nS</u>	<u>+3 nS</u>
Minimum Pulse Width	25 nS	20 nS
Edge Placement Accuracy	1 nS	1 nS
Timing Sets	256	256
Phase Selection	Per Channel	Per Channel
Drive Levels	-5V to +15V	-5V to +15V
Detect Levels	-5V to +15V	-5V to +15V
Output Current	60 mA/Channel	60 mA/Channel
Selectable Levels	Per 24 Channels	Per Channel
Programmable Loads	Yes	Yes
Channels Per Card	24	64
Guided Probe	20 MHz	50 MHz

### **3.1.2 Differences and Mitigation**

Technical Working Groups were established, with representatives from the Prime Contractor, Sub-Contractor, and the End Customer to plan for, and work through, the issues encountered during this effort. Great amounts of co-operation were required, with regular meetings and consistent review at numerous locations. Significant amounts of customer furnished equipment had to be provided and supported in the form of multiple test stations in both the old and new configurations, as well as complete TPSs and the personnel to support, maintain, and de-debug the equipment. Testing requirements and acceptance criteria needed to be developed, and agreed to by all parties involved, and results were to be evaluated and comprehended... When problems were encountered, recommendations were made that required trade offs be considered. Of the three instrument replacements, this required the greatest amount of cooperation effort from the three parties involved to insure a successful completion of the replacement program.

As the project progressed, some differences were identified that were omitted in the design. These mostly included areas where TPSs took advantage of undocumented performance or features that existed in the M895. Every effort was made to address these discrepancies, but some required that modifications be made to the TPS.

The software of the M895 provided undocumented register level access to the hardware. The ability to read and write hardware specific registers was used extensively in the self-test for the M895. Due to changes in the design, the old register map was invalid for the new system. In cases where equivalent functionality existed in the new hardware, the new software emulated the old function. This could not be achieved in all cases.

There were a series of issues that involved differences in the two electronic pin sets. These consisted of differences in the leakage current and characteristic impedance of the digital pin. There were also TPSs that depended on the state that the channel floated to when left in a high impedance state. Although there was no specification for the float state, it was consistently based on the design of the discrete elements of the pin electronics. The new design was also consistent, but the typical level was different from the M895. Another area that has caused problems in compatibility was the performance of the system beyond specification. The specifications for the M895 were based on the design and qualification of that design. The hardware often exceeded the specification in areas such as tolerance to voltage conditions. The newer design, based on the technology, was not as tolerant of these conditions, and would cause TPSs to fail, and in some cases damage the M900 hardware. Many of these issues were addressed by improvements to the custom analog ASIC. Those discrepancies that could not be addressed in the hardware or emulated in software required changes to the test programs.

### 3.1.3 Software Replacement

The software requirements were to provide the same operating environment on the new DTU as on the old. This was a requirement at the level of the compiled and loaded test program. In addition, due to obsolescence, the host computer changed from a VAX platform to an Alpha. This required a change to the operating system. The software was ported to the new computer and operating system and provided binary compatibility. The significant portion of the work resided in the run time system and the lower level hardware interfaces.

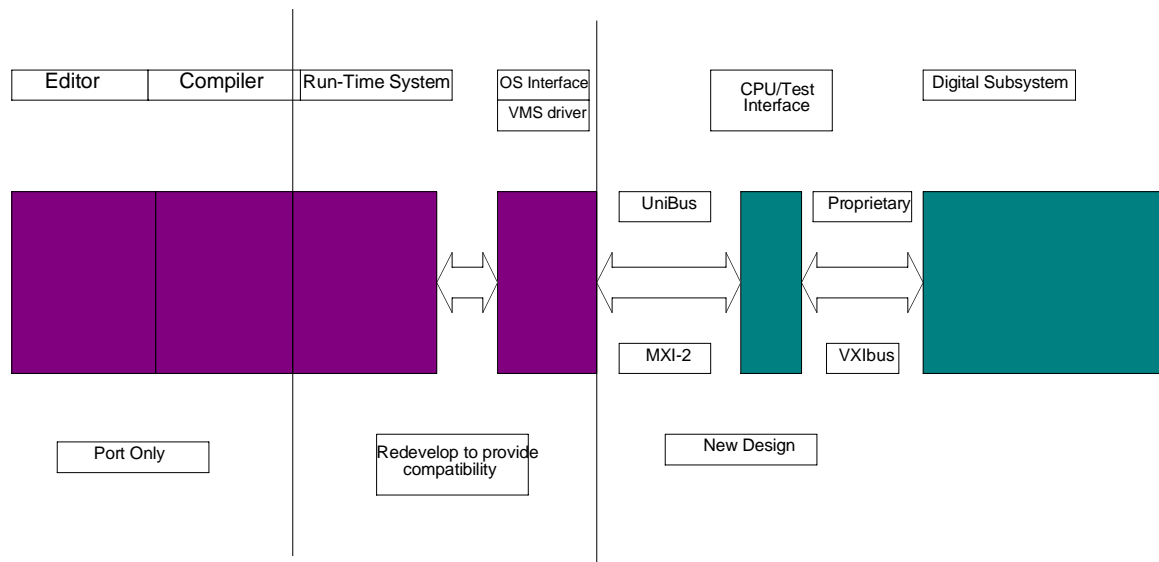


Figure 1. CASS Digital Software Architecture

### 3.2 F-16 Test System Digital Instrument Replacement

In the second replacement, a customer had a requirement for a new version of a test station to support an existing set of avionics from the F-16. The current test set had a

digital capability that could no longer be manufactured due to obsolete parts. In this example, the choice was to purchase a commercial instrument or to redesign the digital instrument with current parts.

The Test program requirements consisted of over 90 TPSs with over 20 ITAs. One company was developing the station and station software while the second had the responsibility to modify and verify the TPSs on the new station. The TPS group performed an analysis of the TPSs for differences in features/characteristics. There was a requirement to limit modifications to the station software (the RTS), or the ATLAS test programs. A limited set of TPSs was selected to verify the new station design. All of the ITAs were verified before delivery using an existing station.

### 3.2.1 Hardware Replacement

**Table 2.** Existing DWG vs. M920 Specifications

Specification	Existing Specification	M920
Number of Channels	24	64
Maximum Data Rate	10MHz	50 MHz
Minimum Data Rate	30Hz	100 Hz
Skew	+/- 10 ns	+/- 3 ns
Edge placement resolution	0.01% of clock or 10ns	1 ns (0-64us) 200ns(64us-0ms)
Phase Resolution	1% or 2ns.	1 ns (0-64us) 200ns(64us-0ms)
Window Resolution	1% or 2ns.	1 ns (0-64us) 200ns(64us-0ms)
Dead time	40 ns	0 ns
Clocks per pattern	16	256
Timing sets	15	256
Channel RAM	4K	32K
Driver Voltage Range	-15V to +15 V	-5 to +15 V (+/- 10 V)
DC Current	60mA	50mA/channel
Output Impedance	30Ω /40Ω source/sink	50Ω/12.5Ω
Detector Voltage Range	VOH -2 to +30 VOL -30 to +2	-5V to +15V
Detector Accuracy	0.2% (70mV max) 2%+ 100 mV	85 mV + 1%
Detector Resolution	10 mV	10 mV
Impedance	> 50 K Ohms	> 50 K Ohms
Load current	1000/100 ohm pull-up/down	1 to 10 mA
Period Resolution	1% or 2ns	1 ns (64us-40 ns) 200ns(10ms-4us)
Period Accuracy	0.01% or 5 ns	0.01% + 1 ns

### **3.2.2 Differences and Mitigation**

During the original evaluation of the instrumentations, several differences were identified. Teradyne held discussions with the system designers and TPS engineers about the potential countermeasures to these differences. The outcome of the discussion was to use the standard products unmodified an account for differences in system software, or the interface to the UUT interface, or if required to change the TPS. This was based on the evaluation of the number of TPSs affected and the estimated level of effort of the change.

#### *Phases and Windows*

The existing system provided 8 timing generators per system that could be used to control either drive or detect timing, where the M920 provides 4 drive phases and 4 detect windows for each channel card (48 channels). To mitigate this difference a mapping scheme from the M920 channel cards to the UUT interface was implemented so that the likelihood of a mismatch was reduced. The TPSs were also scanned to confirm that there were no conflicts. The mapping was adjustable in groups of eight channels to allow flexibility to reconfigure the mapping if desired.

#### *Diagnostic Probe*

The probe on the existing system had different electrical characteristics from the M9-Sereis guided probe. The M9-Series probe was a standard high impedance scope probe, where the older probe has low impedance, around 600 Ohms primarily because the probe was used to source and measure analog waveforms, in addition to digital diagnostics. The M9-series has a buffered output from the probe that could be connected to external instrumentation, however TPSs rely on being able to source signals through the probe and consider the low impedance. The solution was to implement the system with two independent probes and modify the system software to indicate which probe to use.

#### *Voltage Levels +/- 15 vs. -5/+15*

The drive levels for the existing system had a higher range than the M920 could supply. However, an evaluation of the TPSs showed that the critical specification was the + 15 volt rail. The M9-series alternatively supports +/- 10-volt levels, which could cover the lower part of the range for those TPSs that required it.

#### *Pull Up/Pull Down Resistors*

The older DTU had the ability to program pull up or pull down resistors per group of eight pins. The M9-Series can emulate pull up/down resistors using the active loads. This implementation required using two level sets to emulate both the pull-up and pull-down resistors. Because the M9-Series supports two level sets per card, there was enough flexibility in the mapping scheme to support the resistive load without any impact to the TPSs.

### **3.2.3 Software Replacement**

Upon review of the existing commercial technology, it was determined that the hardware specifications for the station fell almost completely within the parameters for Teradyne's M920 product. The use of a *VXIplug&play* driver allowed virtual register level access and the ATLAS interpreter was modified to communicate directly with the M920 rather than the proprietary instrument. Because there were no additional hardware modifications, the systems integrator was able to develop the new software interface without any additional software from Teradyne. This allowed the customer a greater degree of control over the ability to reuse their test programs, including diagnostics without modification.

### **3.2.4 IFTE Digital Instrument Replacement**

In the third situation, a new variant of the IFTE family of test equipment was being deployed. The design of the new system was based on commercial off the shelf test equipment with industry standard architecture. Like the CASS program, there have been a large number of test programs written on the BSTF version of the test station. Therefore, there was a desire to emulate as many of the features of the existing digital capability, but using the commercial version of the M920 instrument. The implementation required some hardware design to map the M920 specifications and features to emulate those of the existing system. In addition, a software component provided a layer on top of the standard *VXIplug&play* driver to provide an interface that corresponded to the existing ATLAS interpreter.

### **3.2.5 Hardware Replacement**

At the beginning of the project, a team of engineers from Northrop Grumman and Teradyne evaluated the performance capabilities of the Northrop Grumman Digital Word Generator (DWG) installed in the IFTE system, and the Teradyne M920 Digital Test Instrument (DTI). The evaluation was based on the specification for the IFTE DWG, and a detailed engineering knowledge of the capabilities of the Teradyne DTI. For most of the performance specifications, the Teradyne DTI met or exceeded the specifications of the IFTE DWG.

Some functional discrepancies were identified and evaluated that would impact the relative compatibility of Teradyne's DTI and the existing IFTE DWG. In addition there were features of the IFTE DWG, which do not exist in the DTI. Teradyne developed an implementation external to the standard commercial M920 that attempted to address these discrepancies with a combination of hardware and software. In some cases, emulation of the performance of the IFTE DWG was based on an evaluation of the intended use of the feature, as opposed to the exact implementation of the hardware in the existing DWG. The result is that the Teradyne DTI performs a very similar function, but does not provide 100% compatibility. Once the implementation for the replacement digital instrumentation was defined, a proposed solution was presented to the Army and

Army TPS developers and support centers, along with representatives from the Air Force, Navy, and Marines.

**Table 3.** IFTE DWG vs. M920 Specifications

<b>I/O Specifications</b>	<b>M920 Specification</b>	<b>IFTE DWG Specification</b>
Bit Rate/Frequency		
15kHz to 50 MHz		
Accuracy	+/-3	0.0025%
Resolution	1 ns	50 ns
100 Hz to 15kHz		
Accuracy	+/-50	0.0025%
Resolution	200 ns	50 ns
<b>Receiver Characteristics</b>		
Resolution:	10 mV	15mV
Accuracy:	+/- (50mV + 1%)	+/-200mV
Input Impedance:	25Kohms +/- 5 %	25Kohms +/- 5 %
<b>Driver Characteristics:</b>		
Accuracy:	+/- (50mV + 1%)	+/-200mV
Drive source/sink capability:	50mA	50mA
Driver slew rate:	0.5 V/ns typ.	0.4/ns min.
Driver Tri-State Switching Time:	20 ns	20 ns
<b>Output Impedance</b>		
Source current	50 ohm +/- 5 ohm	100 Ohms +/- 10%
Sink current	50 ohm +/- 5 ohm	5 Ohms max.

### **3.2.6 Differences and Mitigation**

Northrop and Teradyne reviewed the functional differences with the end customer, identifying the operation of the existing IFTE DWG, and the potential implementation on a Teradyne supplied digital subsystem. The subsystem used the Teradyne standard VXI instruments, but added a series of interface cards to modify the performance and a intelligent software to more closely match the features of the existing system. This decision was based on the large number of fielded TPSs and the risk associated with modifying them.

#### *Tri-State Detection*

The IFTE DWG provides a resistor load to pull the pin to a between state that was used for tri-state detection. The Teradyne DTI emulates the pull-to-between feature of IFTE using the active load. This implementation uses the current sources of the DTI to match the two values of resistors available on IFTE. The impact of this implementation should

be minimal for those TPSs that use the resistive load for tri-state detection only. Those TPSs that uses the resistive loads for other purposes may not function identically.

#### *Match Mode*

IFTE has a match mode that allows the DWG to stop execution when a specified pattern is sensed. When all response pins in the system are in a passing state, the test stops immediately. The Teradyne DTI uses a pipelined architecture to achieve its “high speed” operation. It emulates this operation by “padding” the vectors to allow test results to flow through the pipeline, with a stop instruction on the appropriate vector. This limits the speed of the operation and creates some dead time (time during which no activity can occur) in match mode. The padding vectors use a higher speed timing set to minimize dead time.

#### *Response Pin Impedance*

All low voltage IFTE channels have a 25 Kohm resistor to ground. In addition, every fourth channel has a 100-ohm resistor to ground, with a relay to bypass it. The Teradyne DTI has a high-impedance (>100K ohm). A 25 K ohm resistor was designed into the cable interface boards that translate from the DTI connectors to the Gold dot interface. The 100-Ohm resistor was also implemented on the interface board, and was selectable under software control.

#### *Control Signals*

IFTE provides several control signals that are used to synchronize UUT operation with the tester. The Teradyne M920 has similar capabilities, and both hardware and software schemes were devised to emulate these features. One of the major differences between the designs was the granularity of the control allowed by the system. In the Northrop DWG much of the digital timing was local to the channel card, allowing each card to operate independently with respect to the external control signals. The M9-Series hardware from Teradyne has central control of pattern timing, and local control of pin timing. This allows better performance, but less flexibility.

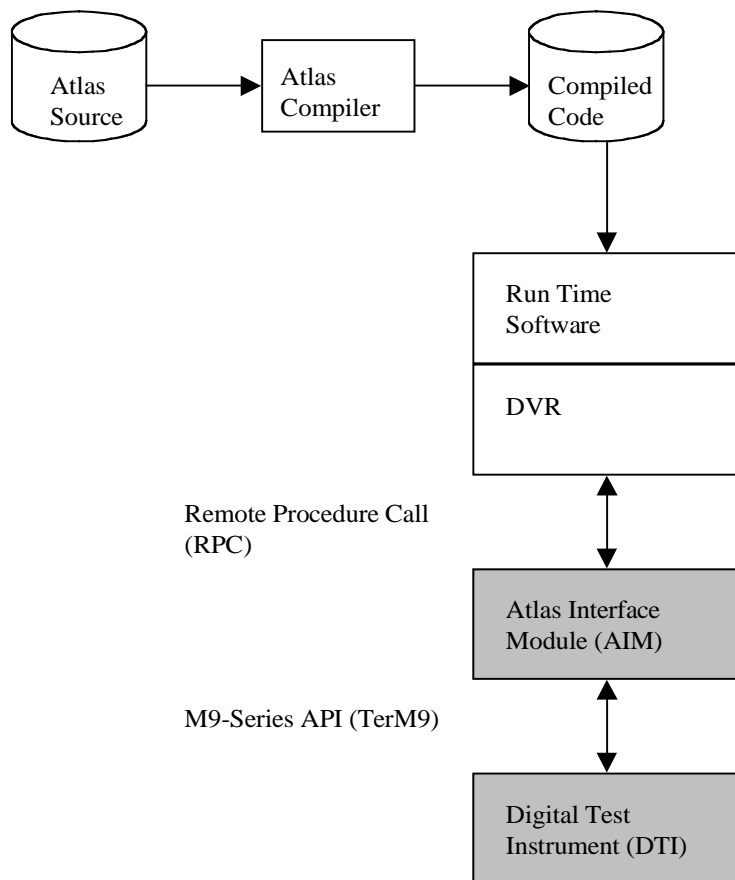
The Stimulus Gate Output and Response Gate Output were driven to a “logic one”, when the test execution starts, to indicate the test was in process. Since timing control signals were different in each mode, the Gate signal was terminated by different timing signals. “Handshake Mode” can be used when testing an asynchronous UUT or one that requires an unknown response delay. This mode was a variation of the static mode but requires an external signal from the UUT that tells the DWG when the response data was available and ready to be sampled. The external clock mode allows the user to use the UUT (or some other external source) to provide a single External Master Clock signal. Stimulus data was sent to the UUT on the rising edge of the External Master Clock. A response was taken on the falling edge of the External Master Clock. Response delay was set by the pulse width of the External Master Clock.

These signals were emulated on the Teradyne central resource board (CRB) by using a combination of existing sync and trigger signals, and external circuit on the cable interface boards. The cable interface boards also provided the mapping from the signals

per card to the CRB. Multiple copies of each of these signals are needed to emulate IFTE (one for each IFTE card). Test programs that use these features may be impacted by slight variations in the timing of the pulses due to the differing implementation. Test programs that use these signals to control precise timing interfaces may have problems.

### 3.2.7 Software Replacement

The requirement for the IFTE system was also based on the need to preserve the investment in TPSs. Therefore the changes were made at the lowest level of abstraction possible. In this case, several of the features of the DWG were emulated in software, and a combination of the Teradyne designed hardware interface and software. The determination was made to replace the Northrop software at the runtime level, with a Teradyne provided interface to the ATLAS system. This module provided the translation from the remote procedure calls from the run time system to the Teradyne *VXIplug&play* driver. The remote procedure calls remained unchanged allowing the TPS to run unmodified.



**Figure 2.** IFTE Digital Software Architecture

