



Optimising test where ICT access is limited

By Amit Verma, Teradyne Inc., USA

 Dans l'adoption de stratégies servant à tester les nouveaux produits, les ingénieurs se basent naturellement sur leurs expériences passées ou sur leurs préférences subjectives sans faire l'analyse quantitative des avantages et des inconvénients des différentes solutions possibles. Il existe des logiciels aidant à choisir les stratégies de tests qui limitent le niveau des coûts de développement et de production.

 Die Ingenieure haben ihre Erfahrungen oder subjektive Vorlieben als Basis für die Bestimmung von Teststrategien für neue Produkte genommen, ohne die Vorteile und Schwächen der verschiedenen Testannäherungen quantitativ zu analysieren. Software für Teststrategie kann dieses Problem überwinden und die Entwicklungs- und Herstellungskosten senken.

 Nell'adozione delle strategie per testare i nuovi prodotti, gli ingegneri si basano tipicamente sulle loro esperienze passate o su preferenze soggettive, senza analizzare quantitativamente vantaggi e svantaggi delle varie possibilità. Esistono software che aiutano a decidere le strategie di test ed a contenere il livello dei costi di sviluppo e di produzione.

A
B
S
T
R
A
C
T

Electronics manufacturers have a multitude of issues to consider when designing process test strategies for their PCBAs; a variety of tools including automated optical inspection (AOI), automated X-ray inspection (AXI), flying probe test (FPT) and in-circuit test (ICT) are available.

boundary scan and digital test environment is a difficult challenge. By using multiple test techniques in a complementary or distributed manner, manufacturers can best achieve their performance goals. Which tools should be used in a distributed test strategy? What is the fault coverage provided by each of the test techniques? How should

tests be distributed to achieve performance goals? What is the correct balance of complementary vs. overlapping test coverage? Which nodes require test access and which do not? What are the risks/gaps in my optimised test strategy? These are the questions engineers are trying to answer in our modern manufacturing test environment.

Each of these technologies has its own fault coverage and performance characteristics that users must evaluate against their fault spectrum and performance goals before determining their test strategy. The loss of ICT test access adds another dimension of complexity to the problem for many modern PCBAs; determining fault coverage and prioritising the nets that require access in a

Glossary

Distributed test

A test strategy that leverages the strengths of various test machines (as measured by their fault coverage, access, test speed, diagnostic resolution or other attributes) in both complementary and overlapping manners to achieve a combined performance that is optimal for the business requirements.

Fault spectrum

The defect type possibilities and the locations where they may occur on a PCBA.

Fault Coverage

The effectiveness of a test stage at detecting a specific defect type on a location that is fully accessible.

Process Test

“Process Test” or “Structural Test” means all test and inspection operations prior to Functional Test. These test and inspection stages are generally focused on verifying correct assembly of the PCB (not functionality).

Test access

The level of access that the test stage has to the PCBA. For example, ICT can have less than 100% access to the signals on the PCBA while transmission AXI can have less than 100% access to the solder joints on a PCBA. The concept of test access is independent of “fault coverage”.

Test coverage

Test Coverage = “Fault Coverage” x “Test Access”

Testability analysis

All available CAD and BOM information is used to determine ICT physical access. In addition, the fault coverage of other test stages like AXI, FPT or AOI are factored in to the test coverage model and tradeoffs are made as to which test stages should provide coverage on which parts and pins. Any lack of access is investigated and test pad requirements are determined based on the fault coverage of all test stages (not just ICT) and the model library information (BSCAN, analog, digital).

manufacturing. Test optimisation and modeling software that enables testability analysis prior to the layout routing stage of PCB design will deliver fewer design iterations, faster time to market, improved fault coverage and lower production test costs.

DfX for boards with limited ICT access

DfX (design for manufacturing and test) is a key focus area for OEMs today because it accelerates time to market and time to volume, reduces manufacturing costs and lowers defect rates. Test strategy software enables test engineers to predict the fault spectrum, plan test strategies, understand fault coverage and test access tradeoffs prior to the layout routing stage of PCB design. Some types of software predict a fault spectrum for every pin, component and signal on the board, and thereby identify which test pads will

The need for test strategy software

How does one develop best practice distributed test strategies? Since each test approach has varying performance levels in many different characteristics, one can easily imagine the evaluation matrix growing to unmanageable proportions - and this means that a modern software analysis approach is required. Without an effective quantitative analysis approach, the high number of choices and convoluted, overlapping characteristics of the different test methods would make optimising a test strategy very difficult and time consuming and lead to questionable results at best.

In the past, engineers often chose test strategies based on past experience or subjective preference. ICT combined with human visual inspection has been an effective test strategy for many years and has been arbitrarily applied to many PCBAs without analysis as to a more optimum test strategy using the new methodologies available today. Modern PCBAs in today's cost and time competitive environment require that we achieve a more optimal test perfor-

mance for each board on a case-by-case basis. A critical requirement for PCBAs with limited ICT access is testability analysis during design, prior to

Ref Des	Part Number	Electrical Type	Circuit Object	Defect	Enabled	Transmission 2D	Analog	Digital
C6	4269-0027-00	CAP	Pin 2	Solder Quality	<input checked="" type="checkbox"/>	Tested	Not Testable	Not Testable
				Missing	<input checked="" type="checkbox"/>	Tested	Not Testable	Not Testable
				Wrong	<input checked="" type="checkbox"/>	Not Testable	Tested	Not Testable
				Skewed	<input checked="" type="checkbox"/>	Tested	Not Testable	Not Testable
				Value	<input checked="" type="checkbox"/>	Not Testable	Tested	Not Testable
C7	4269-0027-00	CAP	Pin 1	Solder Short	<input checked="" type="checkbox"/>	Tested	Tested	Not Testable
				Solder Opens	<input checked="" type="checkbox"/>	Tested	Tested	Not Testable
				Solder Quality	<input checked="" type="checkbox"/>	Tested	Not Testable	Not Testable
			Pin 2	Solder Short	<input checked="" type="checkbox"/>	Tested	Tested	Not Testable
				Solder Open	<input checked="" type="checkbox"/>	Tested	Tested	Not Testable
C8	4269-0063-00	CAP	Component	Solder Quality	<input checked="" type="checkbox"/>	Tested	Not Testable	Not Testable
				Missing	<input checked="" type="checkbox"/>	Tested	Tested	Not Testable
				Wrong	<input checked="" type="checkbox"/>	Not Testable	Tested	Not Testable
				Skewed	<input checked="" type="checkbox"/>	Tested	Not Testable	Not Testable
				Value	<input checked="" type="checkbox"/>	Not Testable	Tested	Not Testable
			Pin 1	Solder Short	<input checked="" type="checkbox"/>	Tested	Tested	Not Testable

Software provides visibility to which defect types within are tested at each test stage. Complementary and overlapping fault coverage can be seen. Reporting is at a component-pin level. Engineers gain visibility on both what is and what is not tested.

Fig. 1 - Fault coverage screen capture from test strategy software

provide the greatest test coverage. By listing the test pads that provide the greatest test coverage in descending order, designers can make intelligent decisions on which test pads should be provided on boards with limited access. The bottom line is fewer design iterations, fewer snags, and improved manufacturing test performance at lower cost.

Complementary and overlapping fault coverage

Some types of PCBAs like airbag or avionics boards that are destined for high reliability applications often require overlapping test coverage to

minimise the possibility of defect escapes. Understanding that no test method is perfect, some OEMs prefer a high level of overlapping fault coverage to ensure all possible defect opportunities are sufficiently screened. Effective test strategy software should enable users to pursue both complementary and overlapping test strategies and to identify the degree of fault coverage overlap in their test plan to meet the quality and reliability requirements of the end use environment.

Test strategies more focused on complementary coverage will tend to deliver higher throughput and lower cost than overlapping test strategies that

verify the same fault types at multiple stages. The optimum test strategy depends on the end use application and user requirements for test access, throughput, cost, and reliability. Test strategy software can help manufacturers understand, quantify and analyse these factors in order to strike a balance that is appropriate for the particular PCBA and their manufacturing business objectives.

Gaps in test coverage

The software should provide insight into what defects are not tested at any given test stage and therefore identify where the test plan is missing coverage

Case studies

Methodology

Three test strategies were applied to PCBAs with limited ICT access using test strategy software. The test coverage and other performance attributes of each test plan were measured on each board using the software's reporting capabilities. Although the software could report test coverage on many types of defects like value, orientation, skew and missing devices, only test coverage on shorts and opens is shown in order to simplify the analysis and demonstrate results.

Analog, Digital and Boundary Scan model libraries were available to the test strategy software to intelligently determine test coverage and eliminate ICT probe access (test pads) in areas where other test stages had overlapping or redundant fault coverage.

Test strategies

Four test strategies were analyzed on each board:

A) ICT only

Description: ICT is the only test method used. ICT utilises maximum access to the board to the degree that is provided by the design.

Strengths: The most common process test strategy used in the industry today. Test coverage is not good when access is limited.

B) Transmission AXI & ICT

(see article on p. 20 of PCE27 for description of this test method)

Description: Transmission X-ray is used to test as many accessible joints as possible on this double-sided board. ICT provides complementary shorts and opens coverage on those pins not accessible by Transmission X-ray and provides coverage on

other component defects like correct part and orientation.

Strengths: Highest throughput, lowest cost, combined AXI/ICT test strategy since transmission X-ray generally operates at triple the throughput of cross-section X-ray. Provides greatly improved test coverage for boards with limited ICT access without sacrificing line beat rate while delivering improved product reliability and reduced field returns.

C) Cross-section AXI & ICT

(see article on p. 20 of PCE27 for description of this test method)

Description: Cross-section X-ray is used to test as many accessible joints as possible (generally upwards of 99%). ICT provides complementary fault coverage on other defects like correct part and orientation but is not focused on opens and shorts testing since AXI provides this coverage.

Strengths: Combined AXI/ICT test strategy for high complexity boards destined for high reliability applications with highly constrained ICT access. Provides highest possible coverage and minimises potential for field returns.

D) AOI & ICT

Description: AOI is used to test as many accessible joints as possible (hidden joints like BGAs cannot be tested). A 2-pass AOI process is used. ICT provides complementary fault coverage on other defects like correct part and orientation but is not focused on opens and shorts testing on solder joints accessible by AOI since AOI provides this coverage.

Strengths: Combined AOI/ICT test strategy for high volume boards with constrained ICT access. Provides good fault coverage at low cost.

Boards tested

Board 1: Double-sided, high density, high complexity - Low

(see fig. 1). It is arguably as important for a test engineer to understand where there is not fault coverage in a test strategy as it is to understand where there is.

Warranty costs, reliability and returns

When engineers can identify where they do and where they do not have test coverage and to what degree that coverage overlaps with other test stages, they can evaluate whether their test plan meets the reliability requirements of the end use environment. Field return rates, warranty costs and customer goodwill costs are substantial

liabilities for all manufacturers; hence delivered product quality level is a key performance metric of any test strategy.

Conclusions

Engineers have used past experience or subjective preference as a means for assigning test strategies to new products without analysing the benefits and weaknesses of various different test approaches in a quantitative manner. Modern PCBAs in our cost and quality competitive environment require a more optimised strategy for each and every PCBA.

Test strategy software tools allow test engineers to predict the fault spec-

trum, plan test strategies, understand fault coverage and test access tradeoffs prior to the layout routing stage of PCB design. The benefits of using effective test strategy software are: fewer design iterations, better test access, improved fault coverage, fewer snags, lower production test costs, improved time to market, improved shipped quality and lower field return costs.

Test coverage more than doubled when using AOI and AXI in conjunction with ICT and production line beat rates varied significantly depending on the test strategy chosen. ✓

Information request no. 3007

volume - Telecom application - Dimensions 16" x 16.5" - 33,325 joints - 3,408 components - 8,044 nets/signals

Board 2: Double-sided, high density, high complexity - High Volume - Computing end use environment - Dimensions 16" x 14.5" - 20,630 joints - 3,250 components - 5,128 nets/signals

Board 3: Double-sided, high density - High volume - Consumer electronics - 3,883 solder joints - 992 components - No BGAs on board - 1,295 nets/signals

Results-software modeling

The results in Table 1 were observed when the board data was modeled using test strategy software. This modeling can be performed prior to the layout routing stage of PCB design so that ICT access can be provided where it is most required, to eliminate overlapping tests, reduce ICT probe count and improve production throughput.

ICT access reduction and fixture cost reduction was greatest in test strategy C for both boards because AXI test coverage is also highest in test strategy C.

Although strategy C delivers maximum AXI test access and maximum combined fault coverage, note that AXI test time in strategy C requires over three times the test time of strategy B.

Although strategy B provides little access reduction over strategy A, fault coverage is significantly improved despite the fact that transmission AXI test access on board 1 and board 2 is 39% and 79% respectively.

Strategy B is preferred for high volume products with cost sensitivity that require improved long term reliability because test time is one-third of the test time in strategy C.

Strategy C is better suited to products that are lower volume, not as sensitive to manufacturing costs and that have a very high field failure cost.

BOARD	1	1	1	2	2	2	3	3
TEST STRATEGY	A	B	C	A	B	C	A	D
% SOLDER JOINTS TESTED AT AXI	N/A	39	100	N/A	79	100	N/A	99
% NETS TESTED AT ICT	83	83	50	90	81	54	90%	67%
% SOLDER JOINTS WITH SHORTS COVERAGE	94	100	100	96	100	100	81%	100%
% SOLDER JOINTS WITH OPENS COVERAGE	41	82	100	46	89	100	68%	100%
AXI TEST TIME [MIN]	N/A	1.0	3.2	N/A	0.9	2.9	N/A	0.8
ICT TEST TIME [MIN]	1.1	1.1	0.8	0.6	0.6	0.4	0.3	0.25
ICT FIXTURE COST	\$31,000	\$31,000	\$20,000	\$19,000	\$17,000	\$12,000	\$5,000	\$3,217

Key points

The use of a combined AXI and ICT method (strategies B and C) on boards with limited test access improves test coverage over an ICT only (A) method.

Strategy D can be very effective in high volume environments for boards with a low number of BGA devices. Test coverage can be greatly improved versus an "ICT only" test strategy.