

Test strategies in the modern SMT production line (part III)

Teamster for global manufacturing

The ever increasing pressures to reduce cost, increase quality and shorten time to market seems an unending task in board assembly. Test strategies can provide advantages by improving the efficiency and quality of processes, and by driving cost reductions and improved performance through the entire product lifecycle. The return-on-investment of an optimized board test strategy can total three weeks improved time-to-market, and over one million euro. Here we can see that there is profound proof for attaining these goals without compromising the product.

The CEM (contract electronics manufacturing) business model has led to an increased focus on assembly process capability that causes OEMs to more clearly measure the cost and quality performance of their manufacturing service providers. Ensuring soldering reliability and products free of assembly defects is the core competency of CEM providers, and a key requirement within the CEM/OEM relationship. Automated inspection methods help to ensure that products are free of assembly defects. They deliver an effective way to verify structural quality as the product moves from one stage in the supply chain to the next.

Manufacturers worldwide are facing shortages of skilled and cheap labor, and the trend toward the CEM model has meant an increased reliance on temporary workers. The companies are looking for test solutions that help to relieve these pressures. Many boards, especially those of high complexity, have to wait a significant amount of time in queue for scarce ICT and FT debug skills. Users are looking for test strategies that can help overcome these constraints and achieve continuous-flow manufacturing, higher inventory turns and reduced WIP. Automated inspection methods can provide ease-of-use solutions by redefining the knowledge base required for test development and debug into solder joint acceptability determination. ICT and FT, on the other hand, require extensive product domain expertise and circuit analysis skills.

The Strategist tool does not imply any specific use model or sequence (order) of tests. The user is free to design a test strategy that employs any number of machines in any sequence or model; thus providing maximum flexibility. The tool performs optimization analysis and test distribution based upon user preferences. These could, for example, prefer one test stage to another, based on its position in the line or restrict overlapping tests on parts. Strategist allows users to associate an independent bill of material (BOM) with each piece

of test equipment in their line to reflect the incremental addition of parts between test stages. Regardless of the recipe, Strategist will help engineers make top-level decisions on what equipment is required in the test strategy to best support the objectives. Then the tool implements the strategy on the shop floor by automatically generating the input files required by each piece of equipment. These files contain information that controls which defects will be tested at each stage.

Teamwork for global manufacturing

Teamwork and effective communication across functional groups in global manufacturing organizations are key elements for worldwide acting companies. Strategist is a vehicle that facilitates teamwork between groups that need to work together to deliver faster time-to-market, lower cost and greater efficiency. It enables test engineers to work concurrently with designers. Engineers can predict the fault spectrum, plan test strategies, and understand fault coverage and test access tradeoffs before the layout stage of

PCB design. The tool enables CEM providers to optimally distribute test coverage within their complementary environment, by helping to understand and quantify tradeoffs related to coverage, throughput, cost and quality. The tool helps to communicate, manage expectations and build partnerships with OEM customers. By quantifying fault coverage and test access on a reference designator pin level and providing insight into test coverage gaps, the tool enables providers to set expectations and evaluate the strength and weakness of different strategies with customers.

Process and test engineers often speak different languages when it comes to manufacturing: the process is often focused on issues related to structural board quality and refers to components by their physical package type, while the test is based on the fault spectrum and refers to components by their function. Because Strategist models both structural and electrical fault coverage and records the physical package and electrical device type of every reference designator on the board, process and test engineers can translate information back and forth between their knowledge domains. An example of this synergy is a test coverage problem on fine-pitch quad-flat pack components in a situation where a process engineer is evaluating a change in the paste stencil thickness from 150 to 200 micron to address lead coplanarity problems on another QFP device. The process engineer is certain that this change will lead to more solder shorts on one QFP, but fewer opens due to the coplanarity problem on the other. By using Strategist to understand the pin-level test coverage at all stages on both of the devices, the process engineer can determine which stencil thickness is preferable to minimize the possibility of defect escapes from test.

Return-on-investment (ROI) model

Test strategies can be leveraged to provide organizations with advantage by improving the efficiency and delivered quality of business processes. Test can be used to gain advantage in a competitive environment by driving cost reductions and improved performance through the entire product lifecycle from design, through product introduction (NPI), manufacturing and warranty. In this way, a use model that leverages the abilities of Strategist can cut costs through many areas of organizations to achieve significant savings. The

Summary of total savings

(Quoted in euro and shortened time-to-market. Note that quality cannot be tested-in in a product, but is resulting from manufacturing processes)

Fewer design iterations, faster testability reviews	€23,000	8 days
Faster NPI	€30,000	13 days
Reduced material and fixture costs and scrap	€275,000++	
Reduced Production Test Costs	€550,000	
Shorter cycle times, improved inventory turns and utilization	€++	
Higher delivered quality, lower warranty costs	€200,000	
Total Savings	€1,077,400++	21 days

savings derived in any particular manufacturing environment need to be studied on a case-by-case basis.

Design iterations, testability reviews and time-to-market

Testability reviews tie up the valuable time of both board designers and test engineers. Manual testability analysis can go through several iterations and lengthy manual review cycles due to mistakes, communication gaps and inconsistencies due to lack of automation and simplicity. The experience level of the individuals involved can have a significant impact on the time required and number of iterations for the review (can triple the requirements). Software that enables efficient testability analysis, planning and facilitates communication between designers and engineers prior to layout routing, will save the time of both, produce fewer mistakes, increase the quality of the testability analysis and improve time-to-market.

A manual testability analysis for a complex board, by a "somewhat" experienced team of engineers, can easily occupy 4-man days between the designer and test engineers combined and go through at least two iterations if not more when errors are later discovered. Strategist can reduce the time it takes to perform testability analysis from 6 days to 3 days. That's a reduction of 3 days or €2400 at €800/day engineering labor rate. Most importantly perhaps is the quality of the testability analysis. The more thorough, automated and effective analysis supported by the tool can eliminate the need for costly and lengthy redesigns later in the product life cycle due to errors, miscommunications or inappropriate assumptions via a manual analysis approach. The impact of a redesign later in the life cycle can easily cost 5 days time-to-market and €20,000 in labor and scrap material costs.

Manual testability analysis

First revision: 4-man days, then second revision: 2-man days

End result: 6-man days labor, suspect quality due to errors, prone to costly and lengthy redesign if errors are significant and discovered later. Additional 5 days delay and €20,000 cost assuming redesign is necessary

Strategist testability analysis

First revision: 2-man days, then second revision: 1-man day

End result: 3-man days labor, higher quality, much reduced risk of redesign

Net savings: €2400 or 3-man days labor

Additional 5 days faster time-to-market and €20,000 saving (assuming re-design avoided)

Strategist can be used to develop fixture-less verification solutions for NPI to complement a traditional bed-of-nail test later in the pre-production stages. This improves time-to-market by eliminating fixture-build time, fixture revisions and debug time that can easily total 8 days for a complex board. Customers can also reduce the number of NPI fixture revisions, improve their NPI fault coverage and improve their time-to-market. Assume

one less fixture required for NPI and eliminates cost of fixture revisions; this delivers €30,000 saving. Eliminate delay time due to fixture build and debug: 8 days faster time to market. Improved NPI test coverage due to improved testability analysis during design cycle can deliver 5 days shorter time-to-market due to reduced debug, repair cycles and wait time. Strategist can reduce the board material costs by eliminating the need for unnecessary test pads. Because the tool can model test coverage before the layout stage of the PCB, engineers can remove unneeded test pads, gain greater density and perhaps even reduce the board layer count. Savings could be substantial depending on the PCB type: typical 5% will deliver approximately €270,000 in material savings per year.

ZUSAMMENFASSUNG

In dieser dreiteiligen Serie (publiziert in den Ausgaben 11/12 (2002), 1/2, und 3/4 von EPP Europe) steht die Organisation von Teststrategien in der Baugruppenfertigung im Mittelpunkt. Dabei geht es nicht nur um den erstrebenswerten Datenaustausch zwischen Design und Fertigungsprüfung in der Produktdefinitionsphase für Concurrent Engineering, sondern auch um das später relevante Test-Konzept im Prüffeld, das sich im Bedarfsfall auf alle verfügbaren Verifikationsmethoden stützt. Der Vorteil richtig gewählter Prüfstrategien: Kosten können weiter gesenkt und die Qualität sowie Zuverlässigkeit der Baugruppen besser verifiziert werden.

RESUMÉ

Cette série de trois articles (publiés dans les numéros 11/12 (2002), 1/2 et 3/4 de EPP Europe) est consacrée à l'organisation des stratégies de test dans la fabrication de sous-groupes. Il n'est pas uniquement question de l'échange de données que l'on souhaite le plus précoce possible entre la conception et le contrôle de production dans la phase de définition du produit pour le Concurrent Engineering, mais également du concept de test ultérieur, au banc d'essais, qui fait appel, si nécessaire, à toutes les méthodes de vérification disponibles. L'avantage des stratégies de test bien choisies réside dans la possibilité de réduire davantage les coûts et de mieux vérifier la qualité et la fiabilité des sous-groupes.

SOMMARIO

In questa serie da tre componenti (pubblicata nelle edizioni 11/12 (2002), 1/2, 3/4 della EPP Europe) l'organizzazione delle strategie di test all'interno della produzione di gruppi costruttivi si trova al centro dell'attenzione. Qui non si tratta solo di uno scambio di dati precoce auspicabile tra design e controllo di produzione nella fase definitiva dei prodotti per la Concurrent Engineering, bensì anche del concetto di test rilevante in un secondo momento nel campo di controllo che, all'occorrenza, si basa su tutti i metodi di verifica. Il vantaggio di strategie di controllo correttamente scelte: i costi possono essere abbassati ulteriormente e la qualità nonché l'affidabilità dei gruppi costruttivi possono essere verificate molto meglio.

This three-fold series on board test and inspection technologies has been presented in the issues #11/12 of 2002 and 1/2, 3/4 in 2003 of EPP Europe. The overview is based on information provided by Teradyne Assembly Test group, and derives primarily from a paper of AXI and test strategy expert Amit Verma.

The tool can reduce ICT fixture costs by reducing the number of nails/probes required if a complementary strategy is chosen. Typical savings are approximately €5000. In addition, it can reduce the amount of scrap generated by the assembly process through improved diagnostic resolution. Because of better testability analysis and planning, defects can be more accurately and immediately pinpointed without as much opportunity for incorrect diagnoses that lead to unnecessary reworks cycles and scrap (savings ++).

Reduced test costs and shorter time-to-volume

Depending on the type of strategy, the tool can reduce verification time by 10 to 30% through the elimination of unnecessary overlapping test. This reduction in time can be achieved at any or all test stages in combination. This reduced test time can significantly improve production efficiency and potentially reduce capital equipment investments. Typical savings are approximately €50,000 per year.

Depending on the strategy, improved fault coverage and diagnostic resolution achieved through better testability analysis and planning will lead to reduced time. Boards can spend a significant amount of time waiting for scarce debug skills at ICT or functional test. For complex PCBAs, debug and diagnosis times can be 5 to 10-times longer than actual test times. In this way, Strategist can reduce the level of WIP and RIP on the shop floor and increase inventory-turn rates by significantly reducing board cycle times. Typical savings are approximately €500,000 per year.

Cycle time, inventory and equipment utilization

Depending on the type of strategy, the tool can reduce the amount of high skill level debug required for the disposition of boards that fail at ICT or FT. Because highly skilled technicians are scarce, the queuing time while boards wait for debug can account for a large proportion of the total product cycle time and create high levels of WIP and RIP. Because of improved testability analysis, planning and decisions to pursue test strategies with better diagnostic resolution, product cycle times can be significantly reduced. Strategist can therefore help to improve inventory turn rates and equipment utilization while reducing WIP and RIP on the shop floor (savings ++).

Depending on the strategy, improved overall test coverage achieved through better testability analysis and planning will support higher levels of quality and reduced warranty and field return costs. Typical savings are approximately €200,000 per year. Intangible customer goodwill costs are also saved and higher customer satisfaction is achieved.

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→ EPP EUROPE 189