

Verification of board assemblies populated with low-voltage IC technologies

# In-circuit test meets next challenges

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*The demand for low-voltage ICs has grown significantly in order to satisfy demands for powerful products, smaller packages, reduced power consumption and longer battery life. However, these ICs are increasingly difficult to accurately and safely verify using conventional in-circuit testers. The reasons are the inaccuracy of traditional in-circuit drive/sense pin electronics. Moreover, there is also the great likelihood of violating increasingly tight maximum voltage and current specifications. Performing powered-up in-circuit vector testing is challenging. Testers are needed with independently programmable, high-accuracy driver/sensors, real-time backdrive-current measurement and control, controller and multiple-level isolation capabilities.*

To perform powered-up vector testing of digital components, in-circuit testers use driver/sensor (D/S) pins capable of force input pins to the required logic states, and sensing the resulting logic states of the output pins. The digital pin drivers are designed as low-impedance voltage sources that can typically source or sink 600 mA or more. This voltage source shortly forces nodes on a board to the logic levels required by the test. This technique of temporarily overdriving component outputs to force a node to its opposite logic state is called backdriving. Backdriving is a common and long established method, occurring due to circuit-

design conditions, possible fault conditions on a board, or missing isolation code in the test program.

## Drive and sense accuracy

To successfully test low-voltage technologies, in-circuit drivers must be accurate enough to supply the logic high and low voltages that are expected by the device input pins. Likewise, the in-circuit sensors must also be accurate enough to detect the difference between logic high and logic low voltages on the device output pins.

Most conventional in-circuit testers use a D/S design that consists of a rail driver and a simple comparator. This is a simple design that is low cost and easy to engineer because it consists of readily available commercial off-the-shelf parts. The rail-driver design typically exhibits an output impedance of approximately 5 ohms and a no-load driver error of approximately 150 mV. The sensor in this design will usually exhibit greater than 300 mV of voltage input error.

More accurate in-circuit testers utilize a closed loop, custom ASIC design that greatly improves the accuracy of the driver and sensor resources. These designs are higher cost and require greater engineering effort, but they typically exhibit much lower output impedance (1 ohm or less) and smaller driver/sensor error (100 mV or less).

Either D/S design is capable of adequately testing chip technologies operating at greater than 1.2V under no-load current conditions. It can however become impossible to test IC technologies that are operating at lower than 1.2 V with the simple design due to the inherent inaccuracies in the pin sensor. Even higher voltage technologies become untestable with the simple design under backdriving conditions, because of the high output impedance of the rail-driver pin design.

## Accuracy under backdrive conditions

An analysis of a typical in-circuit test program of a PC motherboard found that backdriving occurred during 17 of the 56 digital device tests, and that 156 events required greater than 50 mA of backdriving current. The median current was 176 mA, the highest event required 600 mA, and the longest duration was 2.5 ms. Backdriving of this magnitude can be problematic on in-circuit testers that use high-output impedance rail drivers because the voltage inaccuracy of the pin driver increases dramatically as backdriving current increases. Figure 1 shows the relationship between backdrive current and driver inaccuracy for both the high-output impedance/rail driver pin design and the low-output impedance/custom ASIC pin design.

The high-output impedance driver design loses accuracy rapidly as backdrive current increases. At 100 mA backdrive current, the driver is no longer accurate enough to test 1.2 V logic technologies. At 200 mA current, the driver can no longer accurately test 3.3 V technologies. When this current exceeds 300 mA, the driver is not even accurate enough to test 5 V technologies. At 500 mA, the high-output impedance driver exhibits over 2 volts of error. In contrast, the low-output impedance driver is accurate enough to test 0.8 V logic technology even at currents of up to 400 mA.

Figure 2 demonstrates the performance of both high-output and low-output impedance drivers captured in a lab experiment under backdrive and non-backdrive conditions. The waveforms show that the high-output impedance driver programmed for 1.2 V only achieves 0.58 V when it is

## Voltage Error vs Backdrive Current

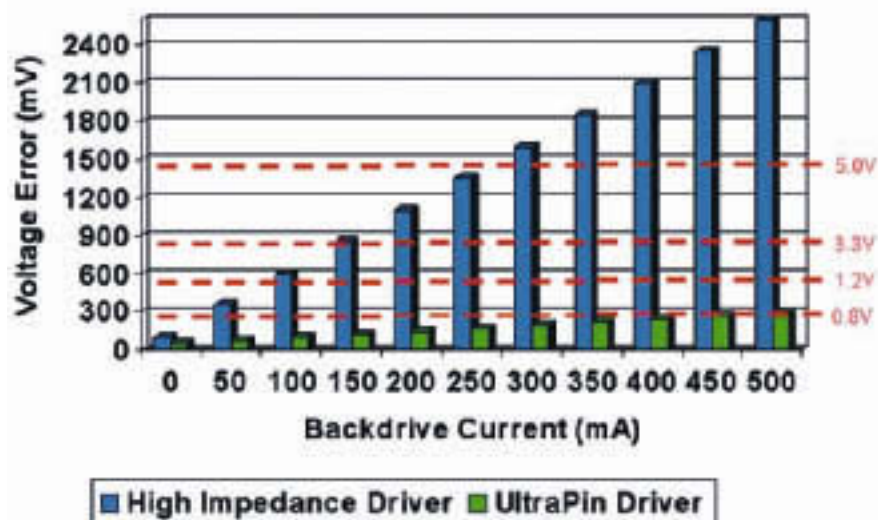


Figure 1: Driver inaccuracy rises as backdrive current increases

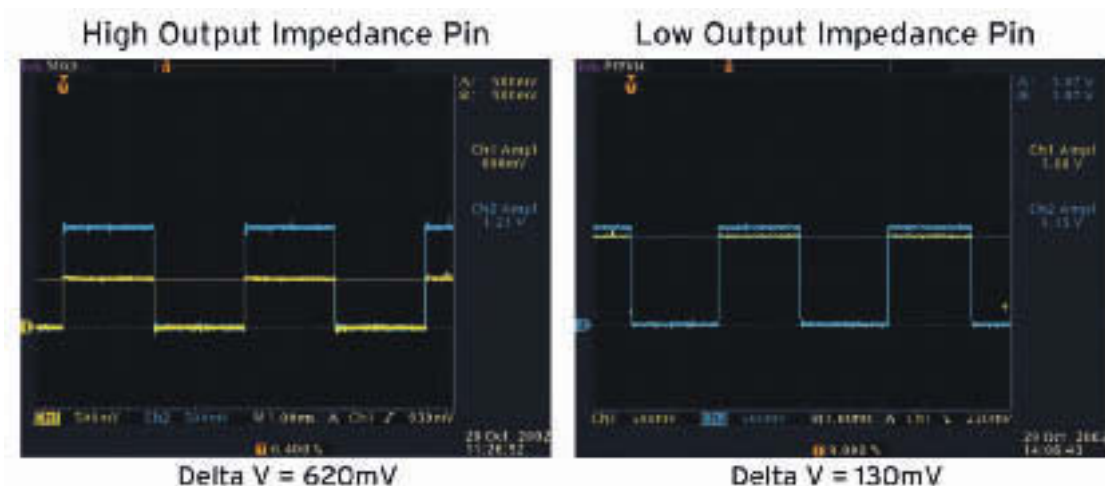


Figure 2: Driver accuracy comparison

subjected to a 6-ohm load. In contrast, the low-output impedance driver is able to achieve 1.07 V under the same 6-ohm load conditions.

### Greater susceptibility to damage

Because of smaller device sizes and lower maximum voltage thresholds, low-voltage technologies are more susceptible to some significant types of failures.

**Gate-oxide breakdown.** The smaller transistor-gate oxide thickness required of low-voltage components makes them more susceptible to damage when they are exposed to over-voltage conditions. The failure mechanism is known as TDDB (time-dependent dielectric breakdown), and it is an interaction between time, temperature, voltage and gate-oxide width. Gate oxide breakdown can occur when a device pin is driven to a voltage greater than its maximum specified rating. For example, the maximal specified voltage rating of Intel's FSB/PSB bus is 1.75 V. If device pins on this bus are driven to voltages greater than 1.75 V for an extended duration, then damage to the transistor gate-oxide will occur.

Most conventional in-circuit testers are designed so that groups of D/S pins must share the same logic-level assignments (groups of 16 or 32 pins are forced to use the same levels). This design is inexpensive, but it can lead to problems when D/S pins in the same group are connected to pins of different voltage technologies. When this occurs, test programmers are forced to use common logic-level assignments for all pins in the group, which can result in some low-voltage device pins being driven beyond their maximum specified voltage ratings.

Over-voltage conditions are also more likely to occur on in-circuit testers that use high-output impedance drivers, because engineers may increase programmed voltages to try and compensate for the voltage inaccuracies that occur when a pin driver is backdriving. Figure 3 shows an example of an application where this possibly could occur.

Advanced in-circuit testers avoid these potential problems by having more accurate D/S pins, and their drivers designed so that assigned logic-level thresholds can be programmed independently for each pin. This per-pin-programmability eliminates test-compromise situations that can cause device

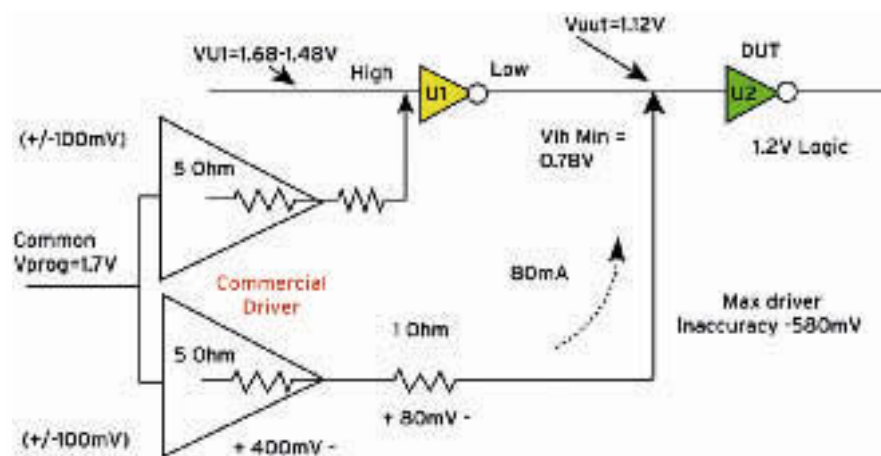


Figure 3: Shared-logic level assignments causing over-voltage condition

Figure 4: ICT report showing backdrive currents

PIN	NODE	NAIL	BACKDRIVE
A3	PICH_HLCOMP	10E	79.06 mA
G1	LAN_RXDI	640	73.79 mA
R21	RSWRST_	90	131.76 mA
NT1	PCLK_ICH	105	84.33 mA
Y20	DVCLUR_I	147	469.08 mA
R22	FERR	614	76.42 mA
C12	CPUNIT_	343	450.64 mA
D11	SB_A2OM_	575	563.95 mA
Y17	SUS_STAT	531	73.79 mA
GCNT_		81	171.29 mA
REF_		67	237.18 mA
SBAD		122	176.56 mA

pins to be inadvertently driven beyond their maximum voltage ratings, and it ensures that each pin on the device is being driven to the exact logic-level thresholds that are required by that device. ESD diode overstress. Overstress at IC-pin circuitry provided against electro static discharge is a failure mechanism that can occur on low-voltage technologies when the ESD protection-diodes are subjected to backdrive currents beyond their maximum. Some chip manufacturers recommend that these diodes not be overstressed beyond 100 mA. Exceeding these ratings can cause ESD diode damage that goes undetected by factory testing, and can be source of latent failures in the field. ICs with

ESD diode-damage lack protection from electro static discharge that can degrade the performance of a device and eventually cause a catastrophic failure. [2] Identifying and avoiding situations of ESD diode overstress is impossible for most in-circuit testers. Currently, only one in-circuit tester on the market is capable of measuring real-time backdrive currents, reporting where backdriving is occurring on an IC, and programing maximum backdriving current and time limits. Figure 4 shows an example backdrive-report from this tester that the operator can use to identify potentially harmful conditions.

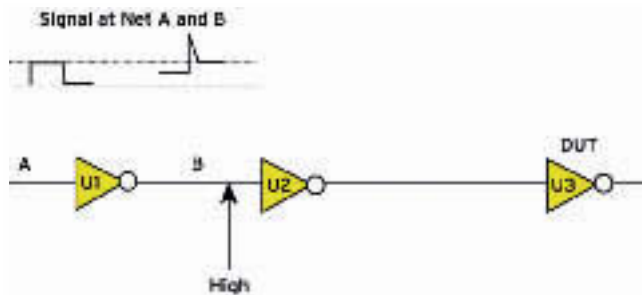


Figure 5: Voltage spike caused by output switching during backdrive

**CMOS latchup.** CMOS latchup is a failure mechanism that occurs when a pair of transistors forms a PNP or NPN silicon-controlled rectifier (SCR) type structure. This results in a low impedance, high-current path from power to ground in the semiconductor. This will cause the device to malfunction or be permanently destroyed. Latchup is usually induced by the application of a fast rise or fall voltage-spike to the inputs of the CMOS device. This can occur due to electrostatic discharge or during in-circuit testing when an output suddenly changes its logic state while being backdriven. Figure 5 shows an application example that can cause voltage spikes to occur on device inputs during in-circuit testing. Figure 6 is a digital-storage scope image that shows the large voltage spike that can occur when outputs change logic state as they are being backdriven, and how this can adversely affect the reliability of the test and the device itself.

To prevent these potentially harmful voltage spikes from occurring during digital in-circuit testing, multiple-level digital-isolation techniques are required. This practice makes sure that all outputs on a net are controlled and are in a known state before connection of a digital driver. Some in-circuit testers only isolate outputs that are directly connected to the inputs of the device under test (DUT), but as figures 5 and 6 show, this is inadequate in preventing voltage spikes which can occur on nets that are not directly connected to the DUT.

## Test duration

Current flowing through a backdriven component increases the temperature of the component's output junction and bond wires remarkably. The maximum safe backdrive time for an IC is a func-

tion of the number of pins on the IC being backdriven, the current level, duration, packaging and technology. Long backdrive times may cause a failure in a bond wire if it raises its temperature above the melting point, or it may activate a fatigue mechanism in the wire that can cause latent defects and early life component failures. [3] Therefore, it is important that in-circuit testers keep test duration to a minimum whenever backdriving is occurring. Advanced testers are designed with specialized digital controller and memory behind the pin architectures that are very efficient at applying test vectors quickly and with precise timing. Conventional in-circuit testers require longer test duration because test vectors are transferred from PC memory during the procedure. Timing for this equipment is very unpredictable because it depends on the type of PC being used, the amount of data being transferred and whatever else may be running on the PC.

An experiment performed to measure the relative performance of the two approaches demonstrated that a tester without a specialized digital controller required 520-times longer than a tester with a specialized digital controller to execute

## References

- [1] Albee: Backdrive Current-Sensing Techniques Provide ICT Benefits. Evaluation Engineering, February 2002
- [2] Diep and Durvary: Electrostatic Discharge (ESD). Texas Instruments Application Report
- [3] UK Ministry of Defense (MOD): Safe Operating Limits for Backdriving. Int Def Stan 00-53/1, November 15, 1991

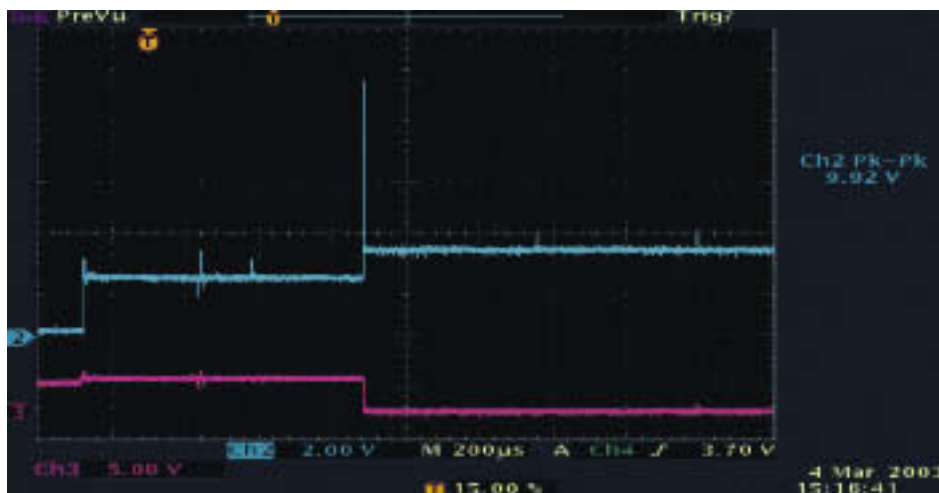


Figure 6: Voltage spike resulting from output changing during backdrive

1000 test vectors (104 ms compared to 0.2 ms). This reduction in execution time results in less stress on backdriven components, and lowers the probability for occurrence of voltage spikes related to on-board activity.

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## ZUSAMMENFASSUNG

Die Betriebsspannung von ICs, früher mal als Standard bei 5 V angesiedelt, wird fortlaufend aus einer ganzen Reihe von Gründen abgesenkt. Das führt jedoch zu Problemen beim In-Circuit-Test von digitalen Bausteinen auf den Boards, insofern die Schwellenspannung für Low- und High-Pegel entsprechend dazu natürlich auch geringer wird und so der Abstand erheblich sinkt. Ältere oder nach konventionellen Maßstäben entwickelte Tester sind hier nicht mehr in der Lage, die Messungen mit der benötigten Präzision vorzunehmen. Zudem kann es auch beim Backdriving der ICs zur Überlastung kommen. Neue Tester-Konzepte weisen weitaus genauere Treiber-Sensor-Elektroniken auf und kontrollieren die Prüfprozedur wesentlich genauer, inklusive der Dauer und Höhe des Backdrivingstroms.

## RÉSUMÉ

La tension de service des CI, autrefois fixée à une valeur standard située autour de 5 V, va baisser pour un certain nombre de raisons. Ceci pose cependant des problèmes pour les tests sur circuit des composants numériques sur les cartes dans la mesure où la tension de seuil pour les niveaux Low et High sera bien sûr également réduite, entraînant une baisse de l'écart. Les testeurs anciens ou développés suivant des critères conventionnels ne sont plus en mesure d'effectuer les mesures avec la précision requise. Une surcharge est également possible lors du backdriving des CI. Les testeurs de conception plus récente présentent des électroniques de pilotes et de capteurs bien plus précises et contrôlent la procédure d'essai de manière beaucoup plus exacte, y compris la durée et la valeur du courant de backdriving.

## SOMMARIO

La tensione di servizio dei circuiti integrati, in passato insediati come standard a 5 V, viene progressivamente ridotta per tutta una serie di motivi. Tuttavia, ciò comporta dei problemi nei cosiddetti In-Circuit-Test di moduli digitali sui circuiti stampati, in quanto a ciò la tensione di soglia per livelli Low High naturalmente corrisponde anche a valori inferiori, consentendo anche di ridurre notevolmente le distanze tra i componenti singoli. I tester più vecchi o sviluppati sulla base di criteri convenzionali qui non sono più in grado di offrire la precisione richiesta per le misurazioni. Inoltre, anche nel Backdriving dei circuiti integrati non sono da escludere dei sovraccarichi. I nuovi concetti di tester ora mostrano sistemi elettronici con driver sensoriali assai più precisi e sono in grado di controllare la procedura di test con una precisione notevolmente maggiore, compresa la durata e l'intensità della corrente del Backdriving.