Teradyne TestStation LX Fault Coverage Comparison Notes for High Net Count Application

Introduction

This document contains observations on the fault coverage observed during a benchmark of the Teradyne TestStation LX vs a traditional in-circuit test program for a high pin count application. The data used for this comparison exercise was derived from the System Test Coverage Reports and actual running of the in-circuit programs and fixtures at the production facility.

Board Overview

Here are some statistics for the target PCB that was being tested:

- The PCB had 8117 nets with valid CAD signal names
- 272 nets did not have physical test access
- 7845 nets were capable of being accessed by an ICT test probe
- The PCB had 7,917 devices (including 3293 Bypass Caps, 1621 Resistors, 1377 Caps, 845 Jumpers, 684 Digital Components and 97 Connectors)

Fixture Details

The 7,845 accessible nets on the target PCB exceeded the maximum pin capacity of both the traditional ICT tester and the Teradyne TestStation LX tester. The traditional ICT system had a maximum pin capacity of approximately 5000 pins while Teradyne's TestStation LX tester has a maximum pin capacity of 7,680 pins.

Because the target PCB net count exceeded the maximum pin capacity of the in-circuit testers, decisions had to be made during program development regarding which nets would be assigned physical test probes and which nets would not be probed. These decisions must be made carefully because removing test access from critical nets can have a significant negative impact on overall test fault coverage and diagnostic accuracy.

To achieve acceptable fault coverage for nodes that do not have physical test access; reduced access techniques that make use of on-board DFT features like boundary scan and drive-through components were employed if available. Using these techniques it is possible to remove test access and still detect gross defects on nets without physical test access, but nodes that do not have physical test access lose some measure of diagnostic accuracy and shorts defect detection.

For the Teradyne fixture, the decision was made to not place probes on board's 857 pure boundary scan nets. These are nets that only connect to boundary scan pins and which could be fully tested using boundary scan Interconnect and Infrastructure tests. There were an additional 68 power circuit nets that were not probed because the electrical loading effect of the probes prevented proper board power up. Finally, there were 256 probes that were removed because of loop back test capabilities that were available in the fixture to test some external 1149.6 nets. Subtracting these nets from the total accessible nets allowed Teradyne to build a fixture with 6,664 test probes that had minimal loss of test coverage and did not exceed the max pin count of the tester.

Since the max pin count of the traditional ICT was much lower than Teradyne's TestStation LX tester, the program developer for that system had to select additional nets where test probe access would not be provided. In addition to the above nets, this programmer decided not to place probes on many non-pure boundary scan and 1149.6 nets, along with some single pin nets that were not deemed critical. Deciding not to place probes on these additional nets allowed the developer to build an ICT fixture with 4414 test probes; but as you will see in the following sections, due to the pin count limitations compromises had to be made in the fault coverage, diagnostic accuracy, and test time when compared to the Teradyne test program.

To remove the electrical loading effects of ICT test probes while running the system boundary scan tests, both fixture developers incorporated a dual-level design. The first level provided contact to all the tester pins and was used when running the traditional in-circuit tests; the second level provided contact only to a limited number of tester pins that were needed to run the boundary scan tests.

Test Time

The total test time to run the target board on the traditional in-circuit test program was 464 seconds (7 minutes, 44 seconds). The total test time to run the target board on Teradyne's TestStation LX system was 180 seconds (3 minutes). It took 4 minutes and 44 seconds longer to run on the traditional in-circuit tester than it did to run on the Teradyne TestStation LX tester.

Further analysis during the program benchmark activities indicated that the Teradyne ICT program was able to run two and a half times faster because it did not need to use time consuming and complicated reduced access techniques to detect board faults. These techniques were used significantly on the traditional tester to compensate for the system pin count limitations resulting in increased their test time and reduced diagnostic accuracy.

Notes on Fault Coverage

The traditional test fixture provided physical access to 4414 of the 8117 valid nets on the target board while the Teradyne test fixture provided access to 6664 of the valid nets. The 2250 additional nets that were nailed in the Teradyne fixture made it possible for Teradyne to detect more faults and provide more accurate repair diagnostics for certain defects.

For example, the mathematical Probability formula for combinations $C(N,K) = N! \div ((N-K)! \times K!)$ can be used to calculate the number of unique shorts combinations on a Printed Circuit Board Assembly (where N is the number of nets on the board and K is the number of nets shorted). Using this formula it can be determined that there are 32,938,786 unique combinations of two pin shorts on a PCB with 8117 nets.

The standard unpowered in-circuit analog shorts test can only detect shorts on nets that have physical test access. Since the Teradyne test fixture provided access to 6664 nets, the Teradyne analog shorts test was capable of detecting 22,201,116 unique two pin short defects. The test fixture for the traditional tester provided access to 4414 nets, therefore the analog shorts test on this system was only capable of detecting 9,739,491 unique two pin short defects. The Teradyne analog shorts test is capable of detecting more than 12 million more shorts than the analog shorts test on the traditional ICT system.

Boundary scan and other reduced access test techniques were used by both the traditional ICT and Teradyne test programs to supplement the analog shorts coverage and to detect shorts on nets that did not have physical test access. These techniques are not as ideal when compared with the standard ICT analog shorts test though, because they take longer to run, require the PCB to be powered up (which can cause electrical over-stress conditions to occur when there are shorts on the board) and the diagnostics messages can be less precise (especially when there is a short to an un-nailed non-boundary scan node). These techniques will also not be able to diagnose shorts on un-nailed nets that are not connected to boundary scan pins.

Additional Analog Components Tested on Teradyne

There were an additional 96 resistors and capacitors that could be tested for value and tolerance on the Teradyne tester but not on the traditional ICT tester because the Teradyne test fixture had physical test access and the other test fixture did not.

There were also 384 capacitors that were part of 1149.6 nets that Teradyne had access to and could perform standard unpowered analog in-circuit tests to verify that the capacitors were the right value and tolerance. The traditional ICT tester and fixture did not have physical access to these capacitors and could only test them indirectly during the 1149.6 tests. The traditional tester could not verify the capacitor value or tolerance.

Additional Component Pins Tested by TestStation LX

There were 79 more pins that could be tested with Teradyne's Framescan FX technology compared to the vectorless test solution used by the traditional test system. This was because the TestStation LX fixture had test probe access to these pins and the traditional ICT fixture did not.

There were also an additional 286 pins that the Teradyne program tested for opens using the BasicSCAN test technique. These pins could not be tested with the traditional ICT tester because the test fixture did not have test probe access and the pins could not stimulated or sensed by a boundary scan pin on the board: