Micro Access Technologies on PCB Assemblies

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IN SUMMARY

As successful as ICT has been over the years in finding potentially costly manufacturing defects early on the production line where it is less expensive to repair, a substantial change has occurred in the characteristics of the tested board assemblies that challenge the continued use of ICT within certain market segments.

In-circuit test has been instrumental in identifying process defects on countless varieties of populated PCB assemblies for over four decades. In-circuit test (ICT) operates by gaining electrical access to the board under test through a bed-of-nails test fixture. The PCB is designed to support this level of testability by incorporating test pads on each net that can be contacted by the bed-of-nails fixture.

When performing component tests, each component is typically isolated from the surrounding components and is tested on an individual basis. This divide-and-conquer strategy allows the system to test virtually any complex PCB without the need for detailed knowledge of the overall assembly's functionality.

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Technology Trends Threatening ICT

High density interconnect (HDI), increasingly higher data rates and miniaturization of PCBs are all trends that limit the widespread use of conventional test pads. With PCB line widths of less than 4 mils and spacing of less than 4 mils on HDI assemblies, it is virtually impossible to place a 35-mil-diameter test pad, or even one that is only 20 mils across.

The increased use of area array packaging, such as ball grid arrays (BGA) and the use of blind and buried vias, also makes it difficult to gain electrical access to signals because the signal trace may be buried in an inner layer, with no available surface access for a test pad. Finally, customers are constantly demanding higher product functionality in either the same or smaller footprint, and this miniaturization trend is also placing pressures on the design community to eliminate conventional test point access.

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Even if it were possible to place test points on a PCB assembly, the added capacitance at the access point location would lower the characteristic impedance of a high-speed, multi-gigabit transmission line at that particular location. For these high-speed signals, changes in the path impedance can cause reflections or other undesirable effects that interfere with reliable signal transmission. As a result, test points may limit the signaling speed that may be reliably achieved on a compromised transmission path and therefore disrupt the target operation of a printed circuit board that has been designed to operate at high speeds.

Fortunately, a variety of micro access technologies are available, including Agilent's bead probe technology [1], Rex Waygood's solder bump [2], Prasad's solder bump [3], Vaucher's access technique [4] and the Test Access Component (TAC) [5], that all offer a means of retaining electrical access on today's complex PCB assemblies.

These techniques, some dating back to the 1980s and 1990s, are in the process of being re-discovered and re-deployed in high-volume production as a means of gaining electrical access on HDI PCB assemblies and on high-speed signal nets. These micro access objects are geometrically small enough to have minimal to no impact on PCB signal routing and minimal impact on high-speed signal integrity.

Changing the Paradigm

Gaining electrical access to PCB nets traditionally involved targeting a large test point or test pad on the PCB under test with a small diameter test probe. This concept alleviated the need to have highly-accurate and expensive fixturing technologies because any mechanical alignment inaccuracies between the test probe and the test pad can be accommodated by using a relatively large test target on the board. Micro access techniques have reversed this paradigm by placing a small test point on the PCB assembly that is targeted by a large flat head or micro-serrated probe. A small feature size object is still contacting a large feature size object in order to resolve targeting inaccuracy, but the locations of the objects have been effectively swapped.

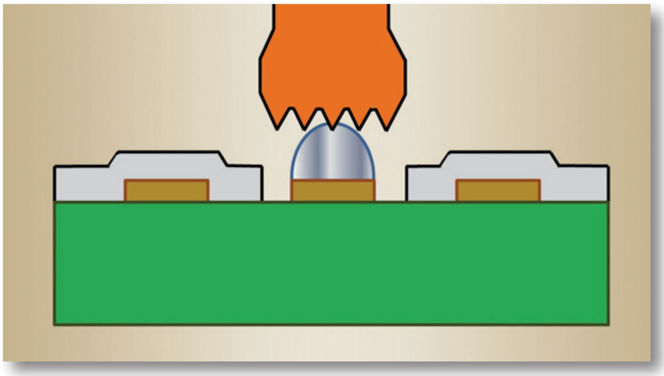

Figure 1: Waygood solder bump, targeted with a large, serrated fixture probe.

A Technology Ahead of its Time

One of the earliest micro access technology dates back to the year 1990 and is cited in Reference 2. This reference describes the concept of using a small solder bump on a PCB to gain electrical access to on-board signals. Specifically, this technique involves printing a sufficient amount of solder paste on a test point location to form a solder bump after reflow that rises above the solder mask. A significantly larger serrated or flat-headed test probe can then be used to contact the solder bump for the purposes of electrical testing of the PCB assembly (see Figure 1).

A second micro access technology published in 1997 (Reference 3), essentially bolsters the earlier teachings of using a solder bump on a PCB as an access point, but discusses placing a solder bump on test point locations that are smaller than 30 mils in feature size.

As interesting as tiny solder bumps are for gaining electrical access to signals on PCB assemblies, there are at least two additional micro access techniques that diverge from this concept.

Getting the Bump Out

An early, non-solder bump micro access technique was disclosed in 1996 at a technology conference (Reference 4). The concept disclosed opening a small aperture in the solder mask directly above a signal trace.

The exposed conductor is contacted by a large diameter, deformable Z-axis conductor tipped probe. The Z-axis anisotropic conducting probe tip material is comprised of a deformable insulating material (similar to an eraser tip) that is loaded with small diameter metal wires that enable electrical conduction in the Z plane (Figure 2). In practice, enough probe force is exerted upon the probe tip to partially deform, enter the aperture opening and make electrical contact with the exposed etch below. The other side of the probe tip is connected to the spring-loaded test probe to maintain the electrical path.

The probe tip geometry is large as compared to the solder mask aperture opening to ease the test fixture's targeting accuracy and repeatability. In practice, the exposed etch is typically HASL finished to eliminate oxidation of the copper etch. The interesting part of this board probing technique is that the PCB signal traces can be laid out without the need to re-route around traditional test points. Needless to say, only signal traces that reside partially or completely on the outer PCB layers can be accessed. This is a common trait of many micro access techniques.

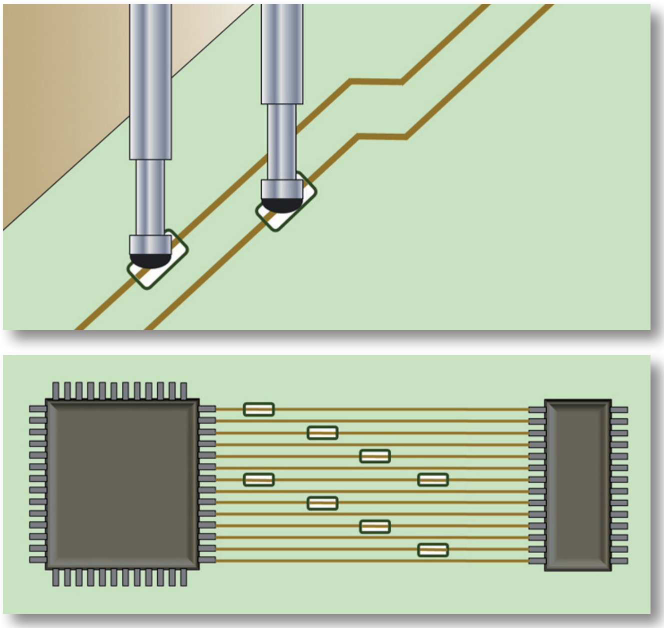

Figure 2: Vaucher concept of using a deformable Z-axis anisotropic conducting material on probe tips to gain electrical access on signal nets through small solder mask openings.

The next non-solder bump micro access technique is called the Test Access Component, or TAC [5]. With this technology, a small surface mount component is mounted directly on top of the signal trace to gain electrical access. The part that is being used as an access point is typically an inexpensive 0402, 0201 or even a 01005 resistor component. Ideally, the part chosen has a body width that is nearly the same width of the signal etch so as to add a negligible amount of additional per-unit-length capacitance to the trace. The signal trace runs directly under the component, effectively shorting out the end caps. As a result, the specific value of the component does not matter in this application.

The TAC device supplies two access locations on the end caps for increased electrical and mechanical reliability. The small component is typically contacted by a large flat head or micro-serrated probe in the test fixture, thereby minimizing the need for highly-accurate fixturing technologies. In practice, a small amount of solder wicks up to the top of the end caps and it is this material that the large fixture probe contacts (Figure 3).

The insertion loss of a 2.5 inch length of 8-mil-wide etch with a 0201 TAC mounted in the center of the trace has been characterized. The insertion loss, or S21 loss of 6dbV at 20GHz, is due almost entirely to the dielectric loss of the FR-4 material and not the test access component itself.

The test access component was additionally tested for mechanical robustness. With this test case, a 0201 TAC was repeatedly contacted with a large 0.060 inch diameter flat headed probe with a spring force of 5 oz. Kelvin resistance measurements were made on each contact cycle and the minimum and maximum values for every group of 100 readings were charted. The results showed that the contact resistance is very low and repeatable at 12 milli-ohms with no open or high-resistance cycles for 100,000 cycles.

Finally, Figure 4 shows a section of the test board and the corresponding TDR measurements for the signal etch and the TAC. As shown in this illustration, the impedance is nominally 50 ohms and dips slightly by less

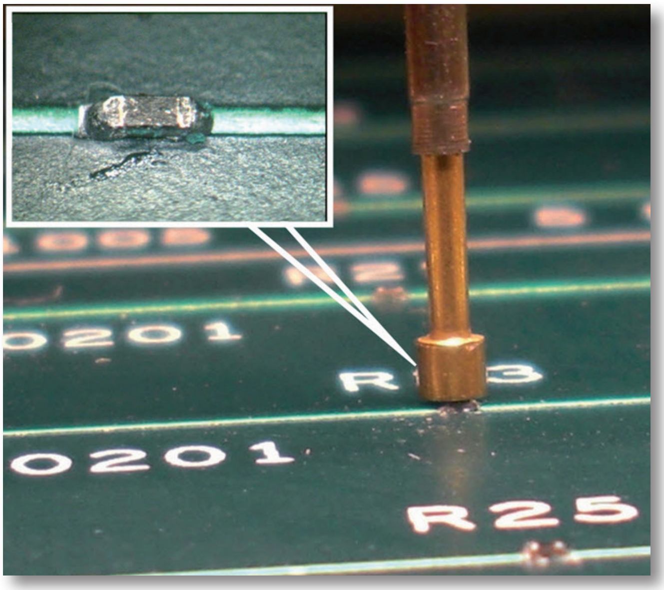

Figure 3: Test Access Component (TAC) used to electrical gain access on PCB trace.

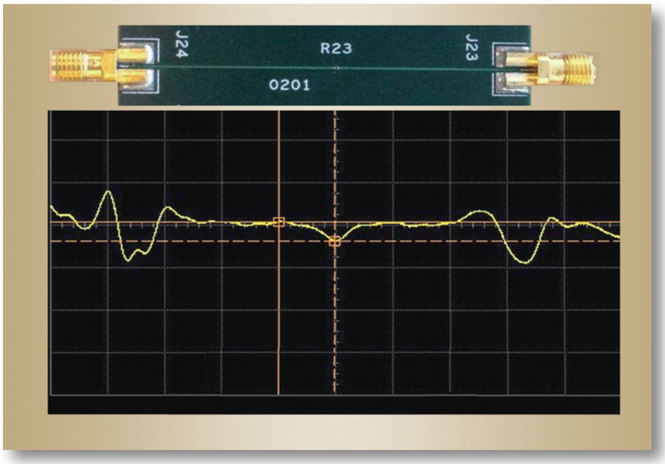

Figure 4: Section of a test board and corresponding TDR of trace with 0201 TAC in the center of 2.5 inch long, 8-mil-wide, 50 Ohm trace.

than an ohm at the TAC location. This slight dip is far less than the normal tolerance of a controlled impedance PCB, which is usually specified as +/-10% of the desired characteristic impedance. As a result, a small test access component can be used on gigabit signal traces with negligible signal integrity impact.

A World of Compensation

Although some signal integrity engineers may try to dissuade board designers and test engineers from placing test pads on high-speed signals, there are ways that the board designer can compensate for the added capacitance of such a structure and create a more uniform transmission line. This technique can also be applied to TAC components that are physically much wider than the signal trace width and add unwanted capacitance and corresponding impedance discontinuity on the line.

Compensating a test pad or a large TAC can be accomplished by removing sections of the reference plane that lies directly below the surface signal trace. In essence, the anti-pad structure in the reference plane effectively removes some parallel plate capacitance and fringing capacitance to best match the nominal per-unit length capacitance between the line and the reference plane. The specific geometry of the anti-pad structure depends upon a number of parameters, including the dielectric constant of the PCB medium, the trace width, height and distance from the reference plane, as well as the solder mask thickness and material. As a result, it is best to model the structure with a 3-D electromagnetic field solver to validate the optimal anti-pad dimensions.

Knowing that the instantaneous return current from an initial wave front propagates in the opposite direction in the reference plane, it is good practice to give the return current a low inductance path to travel. As a result, the compensating anti-etch structure in the reference plane should allow for a return current path directly underneath the test pad or large TAC. Figure 5 shows an example of how a test point can be compensated.

What to Use

Micro access techniques involving solder bumps have been validated as a viable test access vehicle in high-volume manufacturing environments [6]. These structures can be used with HDI PCB assemblies and on high-speed signal traces without negative impact to signal integrity. It is recommended that the solder bump structures be implemented in the manner sited in the published references and to assess any potential intellectual

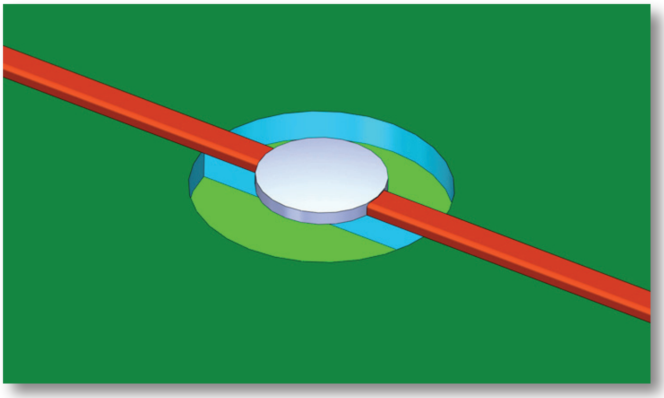

Figure 5: Compensation of conventional test pad's additional capacitance by voiding out two crescent-shaped portions in the reference plane. Note that there is a strip of the reference plane under the test pad for the wave-front return current.

property issues associated with a particular implementation. The other two, non-solder bump access technologies are also viable alternatives that support HDI and high-speed signaling. In the end, it is recommended that all micro access techniques be evaluated to determine which technique yields the best results for a given test application.

In-circuit testing is still viewed by many to be the most economical test method of obtaining the best overall test coverage and diagnostic resolution on contemporary PCB assemblies. PCB trends that involve miniaturization, HDI and high-speed signaling have all threatened the continued use of ICT because of the diminishing use of conventional test pads. Employing micro access technologies on circuit assemblies will help extend electrical access and allow the continued use of in-circuit test platforms to support mission-level testing, as well as future test technologies. **SMT**

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Anthony Suto is a Senior Staff Scientist for Teradyne's systems test group and has worked at Teradyne for over 27 years. In this role, he has contributed in the in-circuit, automated X-ray inspection, semiconductor test and functional test domains. Suto earned his electrical engineering degree from Union College in New York and has authored a variety of patents and technical papers.