POWER *to the* OPENS

As circuit-board complexity increases, identifying structural defects such as opens and shorts represents a significant manufacturing challenge.

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Ever-higher bus speeds and logic densities on today's PCBs (printed-circuit boards) enormously complicate the board-test task. In particular, identifying structural defects such as opens and shorts represents a significant challenge. Today's boards are more likely to contain opens and shorts than did their predecessors, and high node counts make finding these defects considerably more difficult.

In recent years, many companies have turned to a capacitance test as a way to find opens on digital devices during in-circuit test. The technique involves placing a sensor plate on top of the device package to form a capacitor of 10 to 100 fF between it and the board node in contact with the bed of nails (**Figure 1**). (See "How capacitance test works," p. 35.) Unfortunately, the evolution of some board technologies has reduced the usefulness of the conventional capacitance technique. Maintaining bed-of-nails access has become increasingly difficult for designs that include ball-grid arrays, flip chips, and other high-density devices that defy conventional probing. Even when access is theoretically possible, the force required to make sufficient contact to test numerous pins in a small area can exert stresses on the board that can cause damage to the solder joints or to the board itself.

Improving bed-of-nails access to the nodes on the boards has generally involved adding test pads as contact targets, but such test pads occupy precious board real estate. In addition, signal speeds are constantly rising, and adding a test pad to a particular length of signal etch increases trace capacitance, creating a nonuniform impedance for the overall signal path. Such variations along the transmission line can cause reflections and other signal degradation when the board is running in high-speed mission mode.

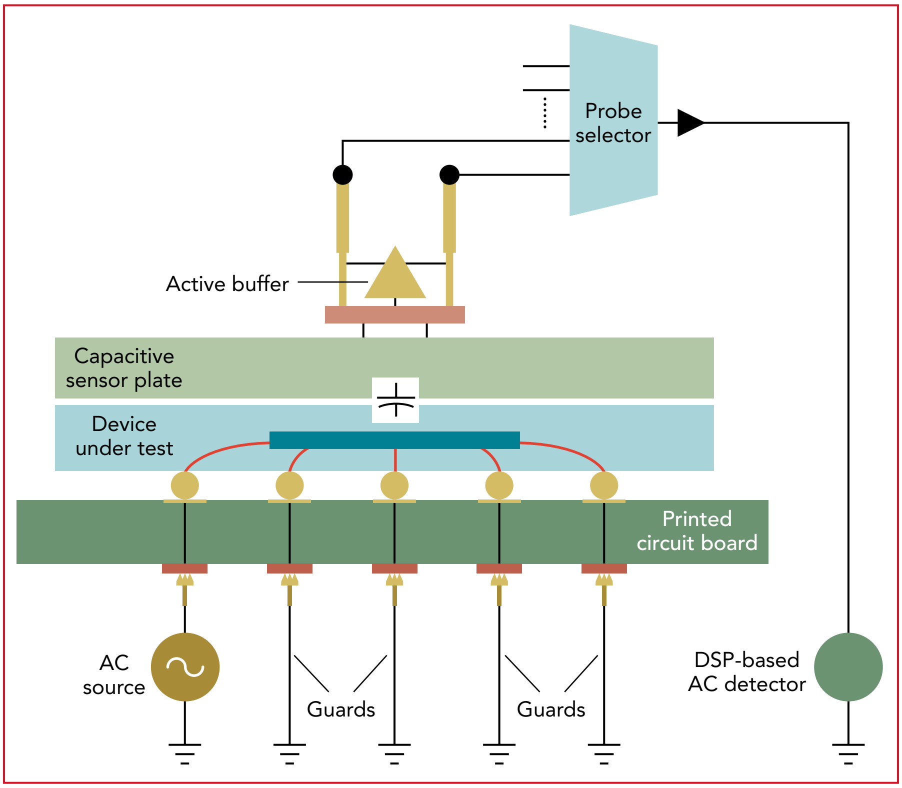

FIGURE 1. A traditional open-pin detection technique employs a capacitive sense plate.

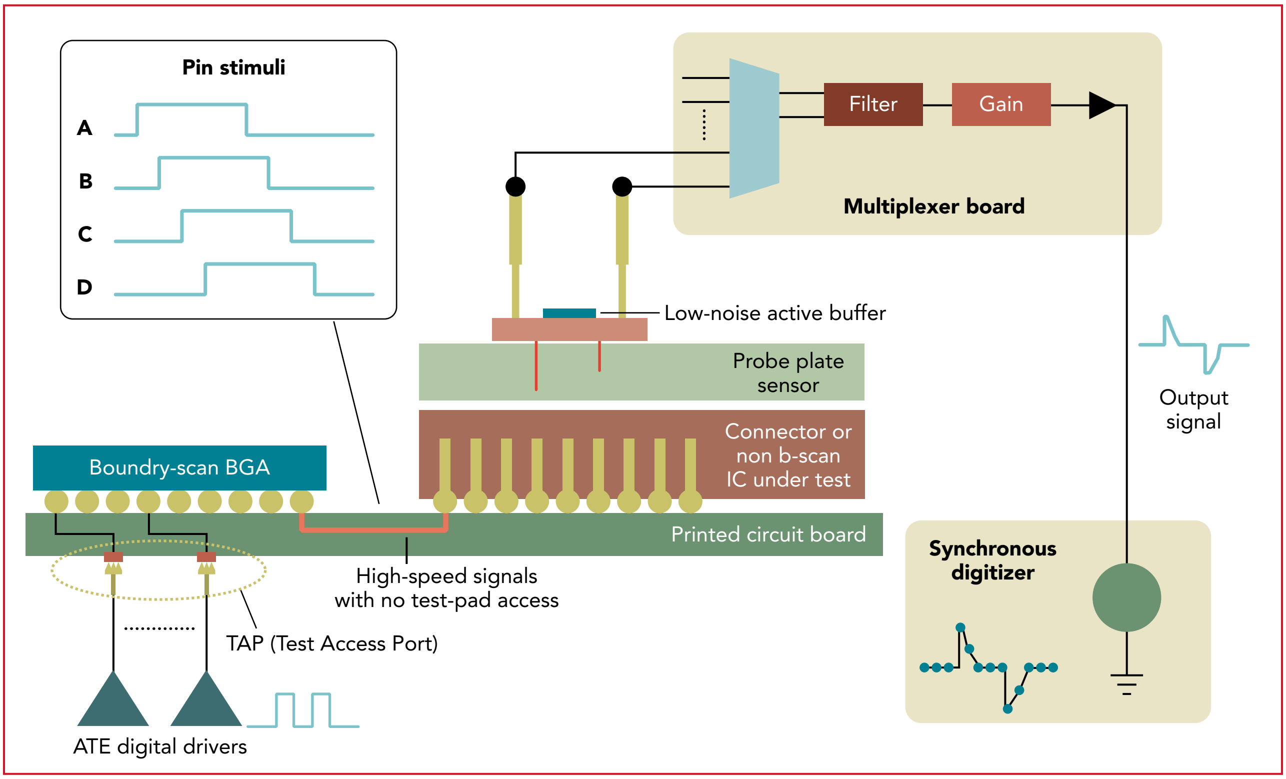

FIGURE 2. The open-pin detection scheme depicted here employs boundary scan as the stimulus source.

Taking advantage of boundary scan

You can improve upon the capacitance-based test by supplementing it with boundary-scan (IEEE 1149) techniques. Many complex devices contain boundary-scan circuitry, allowing access to their I/O structures through a four- or five-pin TAP (Test Access Port). If all devices on a board contain boundary-scan circuitry, the interconnections can be verified using boundary-scan test methods alone. Of course, not all devices offer such a luxury, and the ones that do are often connected to unpopulated connectors or empty sockets during in-circuit test.

Although the boundary-scan circuitry can provide a stimulus signal or measure a response, passive devices cannot interact with the boundary-scan tests designed to locate process defects. A custom test device plugged into the socket or connector could channel the output signal to the tester, but employing such a device proves impractical in high-volume manufacturing. It would increase test time, and the test devices themselves would wear out and have to be replaced.

A more viable option would be to place a capacitive probe in the test fixture over the target socket or connector to easily detect opens between nodes on those devices and a boundary-scan component. The fact that the probe sits on top of the connector or socket rather than being inserted directly eliminates probe or socket wear out. This approach, which I call a "powered-capacitive test," combines the access advantages of boundary scan with traditional capacitive opens detection.

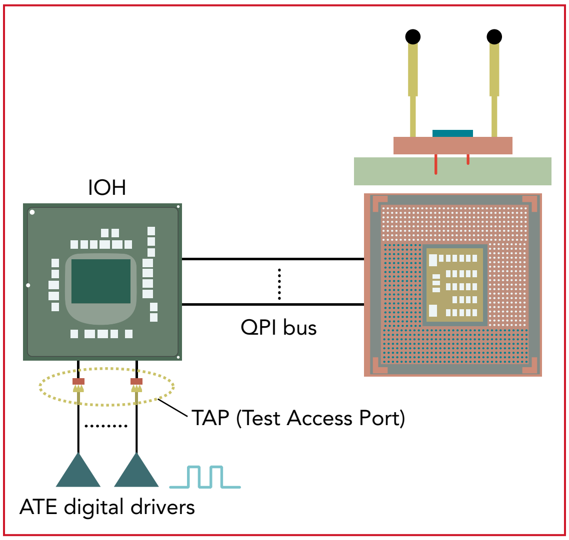

FIGURE 3. In this test example incorporating an LGA 1366 socket and an IOH chip, a TAP connects to ATE digital driver resources that generate boundary-scan commands and stimulus vectors.

The high-level block diagram in **Figure 2** illustrates a test setup for implementing the combined approach. A tester's digital drivers connect to the TAP of a boundary-scan device, providing input signals to the boundary-scan chain that get clocked out of each of the output pins. The output stimulus consists of a single pulse per target-device pin (one rising edge and one falling edge). Whenever possible, all other DUT (device under test) pins are held at a logic-high or a logic-low to isolate the capacitive sensor plate from any other onboard activity.

The signal from the sensor plate is processed through a local low-noise transimpedance amplifier and continuous-time analog filters; it is then digitized, digitally filtered, and finally analyzed. As in a traditional capacitance-based test, comparing the measured signal against thresholds measured on a known-good equivalent identifies any open pins.

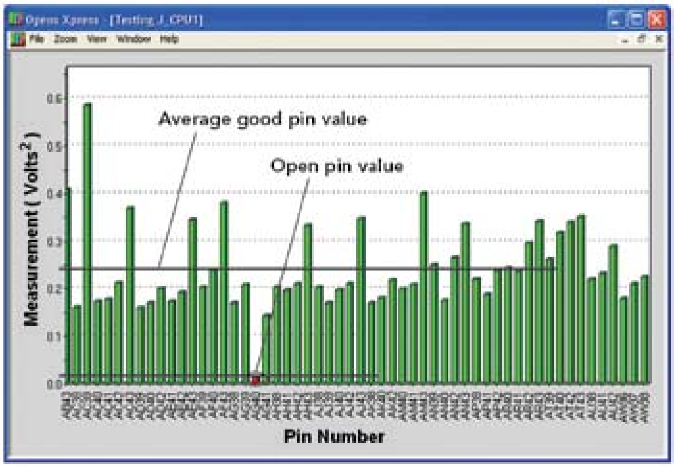

FIGURE 4. These typical test results illustrate the startling difference between a connected pin measurement and an open pin measurement.

Changing domains

To stimulate the board under test, the tester could apply a repetitive signal, such as a square wave, or a single event signal, such as a pulse. Analysis of the output signal could occur in either the time domain or the frequency domain. The powered-capacitive test method applies a nonrepetitive pulse and analyzes it in the time domain, because this combination provides significant benefits over the alternatives during production testing.

Most opens-detection techniques use a frequency-domain approach, applying a sine wave with a frequency that falls into a narrow range—typically 8 to 10 kHz—before taking a measurement. Lower frequencies reduce the capacitive reactance between the probe plate and the component under test, reducing fault coverage. Frequencies higher than 10 kHz can cause coupling between the board and the measurement plate, so a board can pass despite an open pin. This narrow stimulus-frequency range complicates the task of sending stimuli through a boundary-scan chain, because the output square-wave frequency is roughly equal to:

$$f_{\mathrm{TOGGLE}} = \frac{\mathrm{TCK}}{2 \cdot (\#\mathrm{scan\_cells})}$$

where:

- f_{TOGGLE} is the IC pin toggle frequency in hertz,
- TCK is the boundary-scan clock frequency in hertz, and
- #scan_cells is the number of boundary-scan cells in the chain.

The effects of fixture wiring in an in-circuit-tester generally limit the frequency of the boundary-scan clock to 2 MHz or less. With more than 125 cells in the scan path, generating the required 8- to 10-kHz signal becomes difficult. Most devices contain boundary-scan testability structures that can include hundreds of scan cells. Therefore, shifting signals through several such devices can easily require propagation through thousands of cells, further dividing down the toggle frequency.

Even putting all other ICs in a scan path into a bypass mode may not alleviate the frequency problem, because it would not reduce the number of scan cells below the number inside the DUT itself. Although higher tester frequencies are achievable, the necessary specialized fixture hardware would increase fixture costs.

Single-event edge-recognition techniques in the time domain overcome these limitations. A test that uses these techniques does not require a specific test frequency and, therefore, is not restricted by TCK clock frequency. The test simply generates the equivalent of a single pulse with two edges that can be placed anywhere in the vector stream, eliminating frequency-domain scan-cell-length restrictions.

In addition, the time-domain approach works well with all devices that conform to the IEEE 1149.1 and 1149.6 standards, and it does not require boundary-scan devices to support custom commands or fixtures to support additional electronics. Finally, a single pulse offers a throughput

How capacitance test works

A common diagnostic technique for finding opens on digital devices during in-circuit test involves the use of a bed-of-nails tester and a capacitance test. By placing a sensor plate on top of a device package, the tester forms a 10–100-fF capacitor between the device and the board node in contact with the bed of nails. In this technique, a low-amplitude AC stimulus applied to a board node that should be connected to a pin on the device under test propagates into the device and to the plate. A local active probe just above the plate then amplifies this signal and modulates it onto the two wires connecting the probe to the instrumentation via a multiplexer board.

The multiplexer board selects which probe to energize and translates the current signal on the two lines to a voltage equivalent. A continuous-time analog filter removes noise components from the voltage signal. Another function block amplifies it.

Applying a DFT (discrete Fourier transform) to the result removes additional noise components and produces a frequency-domain signal whose amplitude corresponds directly to the capacitance of the circuit path. Measuring that capacitance on known-good boards establishes a baseline for the subsequent production test.

An open on the board acts like an additional capacitor in series with the first. The device leadframe and sensor plate form one capacitor; the pad and trace on the circuit board form the other. The air gap caused by the open serves as the dielectric, producing about 25 fF of capacitance. The equivalent capacitance of the open circuit will be much lower than if the pin were properly connected, unambiguously identifying the defect. The same approach can be used to find opens on unpopulated sockets and connectors as well.—*Anthony J. Suto* advantage over a repetitive test signal. Throughput typically improves by 50% to 400%, depending upon the number of scan cells in the chain and the number of cells that are actually being tested.

Unfortunately, the time-domain technique has some drawbacks. A repetitive signal such as a square wave of known frequency in the presence of noise can easily be averaged over time to reduce the unwanted noise components. Using a DFT (discrete Fourier transform) to measure a single tone, the equivalent noise bandwidth is proportional to the digitizer's sampling rate (Fs) divided by the number of samples (N). Because dimensionally this quantity is reciprocal time, measuring the signal over a longer time produces a narrower DFT bandpass filter with less noise in the measurement. The only downside is the added test time required to integrate stochastic noise to a lower value.

In contrast to a square wave, a single pulse consists of a positive step followed by a negative step that can be spliced together later. Measuring the rich harmonic content in this single pulse requires significantly more bandwidth than is required for measuring the fundamental frequency of a square wave. This additional bandwidth admits additional noise to the system, increasing the measurement's standard deviation, requiring a technique for removing the noise from the signal to make the measurements more repeatable.

Such a technique can be found in the world of radar systems. The method, called "matched filtering" or "optimal filtering," correlates a known signal or template with the measured signal in the presence of environmental noise, as defined by this equation:

$$R(d) = \sum_{i=0}^{K} [(X(i) - Mx) \cdot (Y(i) - My)]$$

where:

- X(i) and Y(i) are the data vectors,
- Mx and My represent the mean values of those vectors, and
- R(d), which is the cross-correlation coefficient, denotes the likelihood that the measured signal matches the reference signal both in temporal response and in magnitude.

Knowing the shape and amplitude of the signal you are trying to detect ahead of time, you can apply a matched filter to significantly reduce the noise components largely attributed to the increased signal-path bandwidth.

Determining whether a node is open requires first performing a de-normalized autocorrelation through the learn process on known-good boards. One way to do this is to calculate a mean and standard deviation from several autocorrelation values and determine whether there is any undesirable variation caused by surrounding noise and whether the magnitude is too small. You should average the learned vectors to create a final autocorrelation coefficient and a reference vector. When the autocorrelation value is compared with the results from the cross correlation during production test, any deviation greater than a maximum percentage or less than a minimum percentage will indicate a defective pin.

In addition, because the board is powered during the test, noise coming from locations on the board away from the node under test can reduce the measurement's signal-to-noise ratio. This phenomenon is common to both the time-domain and the frequency-domain techniques, so you must carefully manage it regardless of which approach you select.

An example

Consider the test setup for the Intel LGA 1366 server-board processor socket shown in **Figure 3**. The left side of the figure shows an I/O controller hub IC (IOH) with boundary-scan capability.

The TAP is connected to the ATE (automated test equipment) digital driver resources, which will generate the required boundary-scan commands as well as the stimulus vectors. A QPI (quick-path-interconnect) bus operating at 6.4 Gbps connects the IOH chip to the processor socket. Without node-pad access, testing this configuration requires the powered-capacitive technique.

The capacitive sensor plate above the LGA 1366 pin field detects the output signals and, in combination with the boundary-scan device, can identify open connections. **Figure 4** shows some typical results; note the significant difference between a connected pin measurement and an open pin measurement. The average of the pin measurements is a little less than 250 mV^2, as shown by the upper horizontal line in the figure. Faulty pin AG40 shows up in this graph as a small red bar. The average connected pin values differ from the open pin value by a ratio of about 10:1. (The data in the graph represent the output value for each pin after processing the raw temporal data through the time-domain algorithms, rather than an amplitude reading that would come from a conventional analog opens measurement.)

The combined key attributes of boundary-scan and capacitive-based opens techniques extends in-circuit test coverage in the presence of limited access to test pads and on densely populated boards that cannot afford test-pad real-estate. Using a single event pulse as a stimulus and analyzing the test results in the time domain eliminates the major drawback of an upper boundary-scan cell limit when testing complex PCB assemblies. Boundary scan and capacitive opens have quietly co-existed for nearly two decades. By giving "power to the opens test," a unique technology marriage will facilitate testing complex boards for years to come. T&MW

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