

## **Teradyne Boundary Scan Product Overview**

Boundary Scan (IEEE standard 1149.1) is a technology that allows silicon manufacturers to design testability into the components that they manufacture. The first commercially available boundary scan components became widely available in 1990. GenRad and Teradyne were the first ICT vendors to supply boundary scan software solutions when the BasicSCAN, Scan Pathfinder, and Victory products were introduced in 1991.

The popularity of boundary scan solutions has grown and now many companies use boundary scan as an alternative or primary testing strategy. Many PC-based benchtop solutions (such as *Acculogic*, *Asset Intertech*, *Corelis*, *Goepel*, *JTAG Technologies*) are now available on the market that can be used by manufacturers and designers to take advantage of the increasing use of boundary scan technology in their electronic board designs.

These benchtop boundary scan solutions can be used in the engineering lab as well as integrated into high volume production test equipment. This is appealing to programmers because a common boundary scan solution can be used to implement a strategy that supports diverse manufacturing facilities. Standardizing on a common boundary scan solution gives manufacturer's the ability to execute the same boundary scan tests regardless of which piece of test equipment they are using on their manufacturing line (in-circuit, MDA, flying prober, or functional). It also simplifies the test developer's job because the boundary scan tests developed for one target machine are portable and can be used on different tester types.

Teradyne's boundary scan strategy is to support their standard BasicSCAN and Scan Pathfinder products as the preferred 1149.1 boundary scan test solutions on the TestStation ICT platform . These Teradyne developed boundary scan solutions have been specifically designed to perform 1149.1 tests in the in-circuit test environment and are tightly integrated with the in-circuit test generators. They use available tester instrumentation hardware to apply the boundary scan test vectors and to increase overall test fault coverage (no additional hardware is required to execute the boundary scan tests).

For those customers who prefer to use one of the available benchtop boundary scan solutions that are available on the market (because they want to re-use existing tests or take advantage of boundary scan capabilities that extend beyond 1149.1), Teradyne offers partnership solutions with select vendors or application level support for third-party boundary scan products. The partnership solutions provide greater levels of integration while the application level support consists of co-authored documentation that describes how to run the third-party boundary scan tests from Teradyne's tester run time and how to install specialized boundary scan instrument hardware and route the signals to the TestStation in-circuit test receiver.

Teradyne has decided not to standardize on a single benchtop boundary scan solution because it is common for our diverse customer base to have different boundary scan vendor preferences and because the boundary scan tools used during product prototyping tend to drive selection of which benchtop boundary scan solution will be used during production testing.

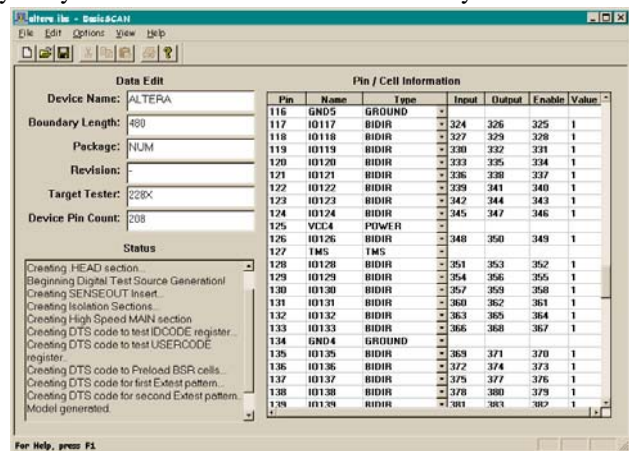
Following is a brief description of the features and capabilities of Teradyne's standard boundary scan products.

## BasicSCAN

BasicSCAN is a software product that automatically generates TestStation digital test models for boundary scan components. Given component boundary scan information, BasicSCAN can generate a comprehensive digital test model in seconds. The BasicSCAN test relies on using tester nails to detect opens on device pins; therefore it is designed for test situations where the tester has access to a majority of the device pins. TestStation's Digital Test Generator uses BasicSCAN models to generate standalone tests for each of the boundary scan devices on the board. BasicSCAN drives the TAP pins of each device directly during the test so it does not need to be concerned with the scan path configuration of the board or how the boundary scan components are connected.

### Capabilities of BasicSCAN include:

- Ability to import device boundary scan description information in either industry standard BSDL format or TestStation's simple IBS file format.
- A graphical user interface that allows easy entry and modification of device boundary scan information.
- The ability to automatically generate a digital test model for Teradyne's in-circuit test systems.
- The ability to generate a BSDL model from information entered into the BasicSCAN user interface.
- Checks for correct Instruction Register capture value and proper register lengths.
- Checks optional component IDCODE and USERCODE values.
- Detects open faults on any device pins that are nailed.
- Checks internal logic of components that support the optional RUNBIST instruction.
- Automatic generation of isolation sections that tell the test generator how to shut off the boundary scan component while testing other components on the board.
- Accurate pin level diagnostic messages.
- Takes advantage of TestStation's powerful Digital Test language features so that no user modifications are required to support these device wiring configurations:
  - ◆ Unnailed device pins
  - ◆ Input pins tied together
  - ◆ Pins tied to power/ground nodes
  - ◆ Output pins tied together
  - ◆ Output pins tied to input pins



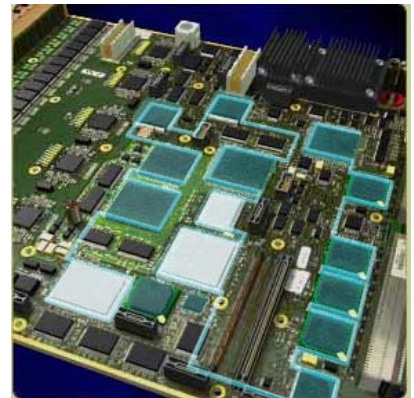
## Scan Pathfinder

Scan Pathfinder is a software product available on the TestStation in-circuit test systems. It is designed to automatically generate and execute comprehensive tests of boards that have boundary scan components and limited tester access. Scan Pathfinder analyzes the board circuit description and BSDL models to determine the scan path configuration and automatically generates a boundary scan test program and diagnostic file. Scan Pathfinder does not require tester nail access to detect targeted faults on the boundary scan nets; therefore it is primarily intended for test situations where the tester will not have access to the boundary scan device pins.

Scan Pathfinder operates the entire scan path(s) as a single unit. Tester nail access is only required on the primary TAP pins of each scan path; access to the intermediate TDI/TDO connections, and the pure boundary scan nets is not required. Scan Pathfinder is integrated with the rest of the TestStation hardware and software and can make use of tester nail access wherever it is available. The tester nails can be used to test analog components, apply test vectors, isolate conventional digital components, detect opens on nailed single pin boundary scan nets, and detect shorts between nailed nets and non-nailed boundary scan nets.

### Capabilities of Scan Pathfinder include:

- Support for boards that have multiple scan paths.
- Automatically generates boundary scan test programs based on detected scan path configuration.
- Automatically generates isolation vectors that can be used to disable all boundary scan devices while executing the conventional in-circuit tests.
- Supports boundary scan test program customization via User Option settings.
  - ◆ Define UUT scan paths.
  - ◆ Define initialization code for scan path selector and bridge components.
  - ◆ Define logic levels used during the boundary scan tests.
  - ◆ Define Nets that should not be tested.
  - ◆ Force values into selected boundary register cells.
  - ◆ Limit the number of tester nails that are used simultaneously.
  - ◆ “Test Using TAP Port Only” option allows generation of fixture-less boundary scan test programs.
- **Hardware Test** verifies the integrity of the boundary scan components.
  - ◆ Verifies that TAP signals are not open or shorted.
  - ◆ Verifies the Instruction Register Capture values of all boundary scan components.
  - ◆ Verifies length of Instruction, Boundary Scan, and Bypass Registers.
  - ◆ Verifies that unique test patterns can be shifted through the Instruction, Boundary Scan, and Bypass Registers.
  - ◆ Verifies values of optional IDCODE and USERCODE registers.
- **Opens Test** diagnoses open pin faults on boundary scan pins that have access to a tester nail.
- **Interactions Test** diagnoses shorts between conventional nodes that have access to a tester nail and boundary scan nets that do not have access to a tester nail.



- **Interconnect Test** diagnoses opens and shorts on boundary scan nets that do not have tester nail access.
- **RunBIST Test** performs parallel device logic testing of all boundary scan components that support the optional RunBIST instruction.
- **Virtual Digital Test** feature allows testing of non-nailed conventional digital component pins using boundary scan pins as virtual drivers and sensors.
  - ◆ Component test vectors specified in simple parallel format using either TestStation's Digital Test Language or Burst Language format.
  - ◆ Analysis software determines which pins can be driven with tester Driver/Sensor nails and which pins can be driven with virtual boundary scan drivers and sensors.
  - ◆ Automatic serialization of isolation and test vectors that require virtual drivers and sensors.
  - ◆ Fast throughput. Test vectors are loaded into the Deep Serial Memory instrument to eliminate digital load time.
- Comprehensive test reports that can be viewed in graphical report summary windows or as text files.
  - ◆ Shows the order of the boundary scan components in each scan chain.
  - ◆ Shows the TAP net names for each scan path.
  - ◆ Shows statistics about the percentage of boundary scan components on the board and the number of nailed and unnailed nets.
  - ◆ Shows the number of potential shorts on the board and how many are detected by each generated test.
  - ◆ Shows the number of potential shorts that are not detected and why they can not be detected.
  - ◆ Shows the overall open pin fault coverage for each of the boundary scan components and specific opens pin information for each boundary scan pin.
  - ◆ Shows pure boundary scan nets (where tester nail access is not required).
  - ◆ Shows unnailed conventional nets (where tester nail access is recommended).
- Separate Boundary Scan Run Time Diagnostic task ensures accurate device and pin level diagnostic messages.
  - ◆ Failing device Name.
  - ◆ Failing device Type.
  - ◆ Failing Nets.
  - ◆ Failing tester nails and boundary scan virtual nails.
  - ◆ List of component pins connected to the failing nets.
  - ◆ Expected and Measured values.
  - ◆ First failing test vector.
  - ◆ Real time generation of Adaptive Patterns to resolve ambiguous faults.
  - ◆ Detects fault conditions on connections between different scan paths.
- Boundary Scan Debug mode allows users to enter commands and view information.
  - ◆ Shows the scan path configuration.
  - ◆ Shows instructions that have been loaded into the boundary scan devices.
  - ◆ Shows values that were loaded into the boundary scan cells.
  - ◆ Shows boundary cells that captured incorrect values.
  - ◆ Shows all boundary register cell information associated with specified component pins or nets.