

# Vector vs. Vectorless ICT Test Techniques

by Alan Albee and Michael J. Smith, Teradyne

Over the last decade, there has been a move away from powered-up digital in-circuit vector testing to unpowered analog-based (vectorless) device-pin opens testing for large and sometimes small digital devices. Two of the driving factors behind this move are the increasingly complex and custom design of digital devices that are being used and the limited digital in-circuit test (ICT) capabilities of most ICT systems. Most ICT systems on the market today simply do not have the timing and voltage accuracies required to reliably and safely test today's generation of low-voltage, high-speed digital components.

At the same time, analog vectorless measurement techniques that can be used to detect open pins have become more acceptable and widespread. The introduction of active capacitive probes and advanced software algorithms has made the open-pin defect detection provided by these techniques acceptable to most manufacturers.

ICT program developers also lack the digital device models required to perform digital vector testing, and they do not have the time required to write digital vector models for complex devices. As a result, many advanced ICT systems also are using analog opens techniques. This has almost leveled

the defect coverage of low-cost ICT and manufacturing defect analyzers with the high-performance ICT systems, although the advanced analog open techniques found on the high-performance ICT systems do give superior defect detection on small-geometry devices.

Some manufacturers no longer feel that they need to verify that the correct device has been placed and that it is functioning correctly. They are willing to settle for analog opens vectorless testing because it can detect structural defects.

All of these factors have combined to make analog opens techniques the preferred solution as manufacturers settle for less test and fast implementation, although there may be potential hidden cost. Costs can arise because analog open vectorless measurement techniques have a number of limitations compared with traditional digital vector testing that have been ignored or forgotten.

## Additional Fixture Costs

Both digital vectors and analog opens techniques require direct, or in some cases indirect, access to each pin of the DUT. As a result, limited access is not really an issue between the two techniques.

Analog opens testing requires that additional hardware be built into the test fixture. The hardware consists of a probe/plate that must be accurately placed over each device that will be tested and a signal amplifier and a central multiplexer/amplifier that interfaces directly with the ICT measurement subsystem (**Figure 1**).

Some test systems also need additional hardware to deal with the signals generated from the fixture hardware, which adds cost to the test system. The additional hardware typically increases fixture costs by \$100 to \$150 per device, and that doesn't include the fixture top gate needed to position the probes on the board.

Fixture complexity and costs further increase if capacitive probes are required for both the top

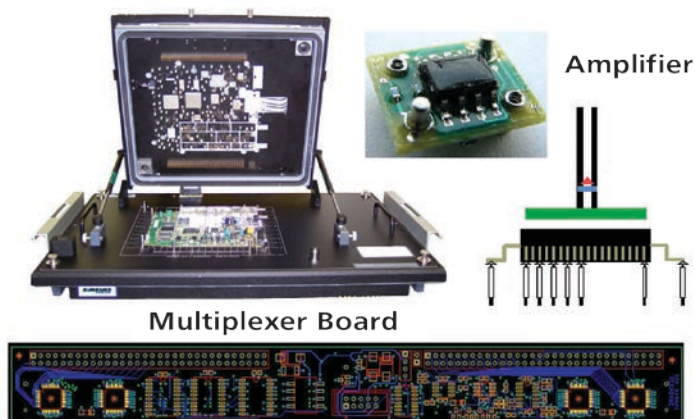


Figure 1. Fixture With Probes Fitted, Amplifier, and Multiplier Card

and bottom sides of the board. In this case, the probes must be designed into the probe plates with CAD systems to get the position and height setting correct. This also can be a problem for bottom-side analog opens probes in a single-sided fixture. These costs quickly increase with 20 opens tests, on average adding about \$2,500 to the cost of a fixture. With vectorless tests, these costs are incurred with each test fixture that is built.

In comparison, powered-up vector tests do not require any fixture hardware. For that reason, manufacturers have the benefit of lower fixture costs and the possible elimination of expensive hold-down gates.

### Additional Fixture Reliability Problems and Maintenance

Including additional hardware in the test fixture decreases its reliability. In the case of analog opens probes, they can be easily moved and damaged during the rigors of production testing (Figure 1). They are not expensive to replace at \$30, but any alignment errors in the probe can produce misleading results, false failures, or false passes as well as potential damage to the UUT. This adds a higher level of fixture maintenance and test uncertainty. And dealing with probes mounted into the probe plates prompts a much higher level of support complexity.

With powered-up vector testing, there is no special fixture hardware required to execute the tests. Reliable test results can be more easily achieved because there are fewer variables that manufacturers must control and less variance across different test systems and test fixtures.

### Throughput

One issue not normally considered is the difference in test time associated with using analog opens techniques vs. digital vector tests. Analog opens typically take about 2 ms per pin to test.

The amount of time required to execute a digital test depends on the number of vectors and the vector rate. An ICT system applying digital test vectors at a 5-MHz data rate (200 ns per test vector) can execute 10,000 test

vectors in the same amount of time it takes to test one pin using the analog opens technique. Digital test vectors also can accommodate multiple pins in parallel rather than one pin at a time. Even accounting for a typical 10-ms vector load time, it is obvious that digital vectors have a significant test throughput advantage compared to analog opens type measurements.

A digital test usually takes less than 50 ms to execute, and the test time is almost independent of the number of pins being tested. A device with 1,000 pins uses about 2 s for the analog opens techniques to complete vs. 50 ms for a digital vector test. As a result, there is a 40x to 50x faster throughput advantage if digital vectors are used.

High-performance ICT systems also can test similar digital devices in parallel; that is, memory devices, again speeding up vector-based test. As manufacturing beat rates increase, the amount of time allowed for ICT decreases. Moving tests from analog opens techniques to digital tests will decrease the test time significantly and either match the line's beat rate requirement or allow additional tests and device programming on the test system.

### Defect Coverage

Typical defect coverage for an opens test is around 85% and can be as high as 99% or as low as 20% depending on the package geometry and construction. Power pins cannot be tested with analog opens techniques and are not always included in defect coverage reports.

Digital test defect coverage normally is very high, especially when boundary scan is used, and we would expect higher than 95% defect coverage. Unlike analog vectorless test techniques, the fault coverage of digital vector testing is not limited by the device package geometry or construction.

Analog vectorless tests utilize a learned

technique, and the fault coverage reports are just estimates of what defects the software thinks the test will detect. Until the defect is actually present on the board and it gets detected, the manufacturer cannot be confident that defects are really being detected. They could have false passes on open pins because of board coupling defects or unguarded nets that do not have physical test access.

With digital vectors, an advanced ICT system can use automated fault injection techniques to determine whether or not open pins are detected. This can give manufacturers confidence that open pins will be detected and diagnosed accurately even before the program and fixture are sent to the manufacturer.

### False Fails and Missed Faults

As with any learned technique, the analog opens technique can lead to marginal measurements that can be close to the limits. Advanced software algorithms in high-performance ICT systems can help eliminate this problem, but many systems use older software that can cause false failures and false passes.

Digital tests, on the other hand, use simple logic ones and zeros, making them less susceptible to false failures. Digital tests also provide additional confidence that the device is working and has power connected to it.

### Digital Pin Electronics

ICT always has been an ideal place to carry out board customization and functional test. Simple programming such as board serial numbers complete

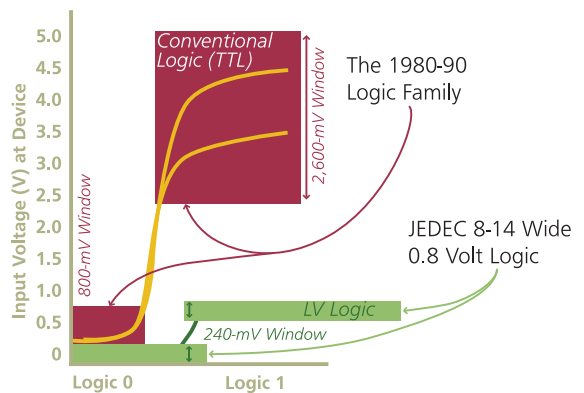


Figure 2. Low-Voltage Signals vs. Traditional 5-V and 3.3-V Logic

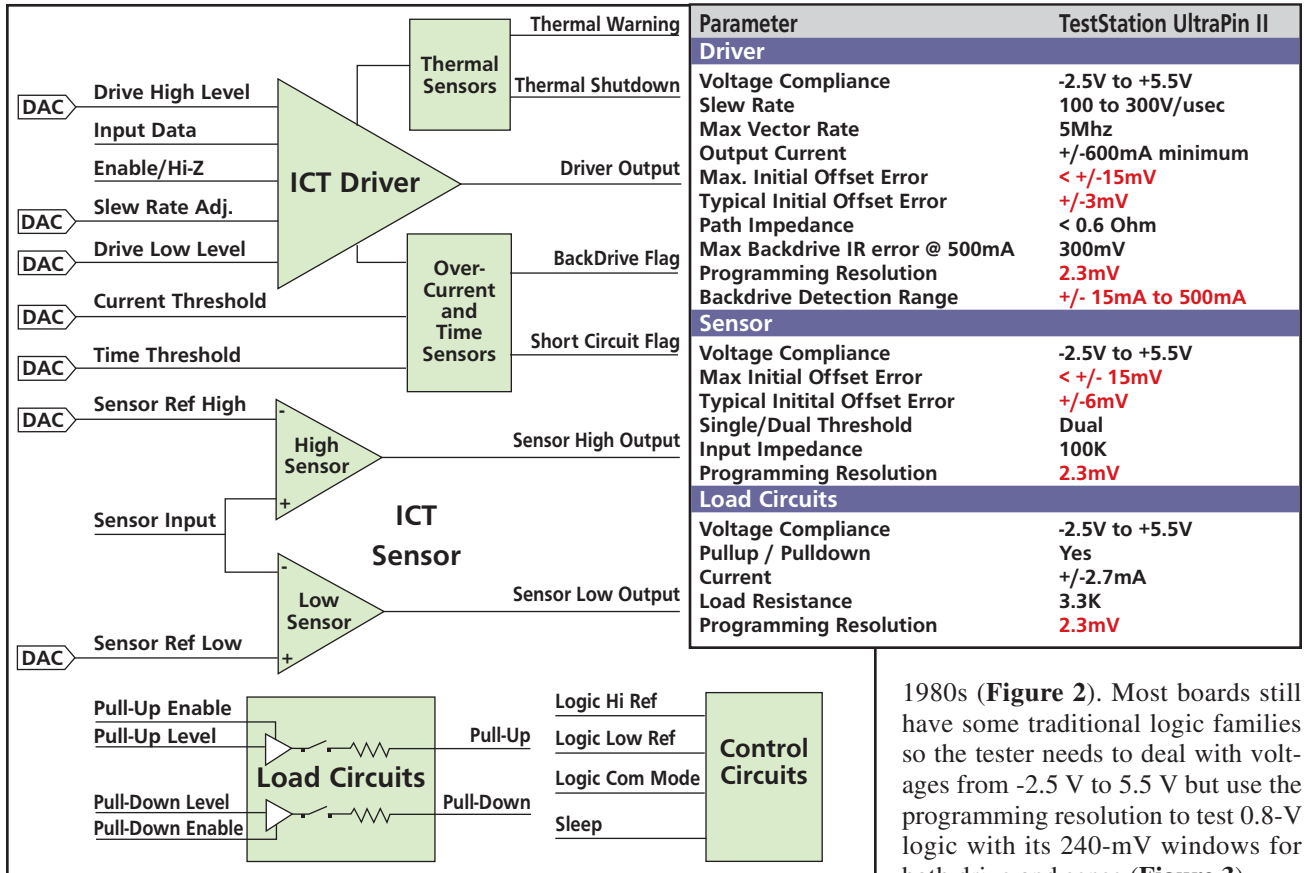


Figure 3. TestStation Pin Electronics

in-system programming, and Flash can be completed at board test but requires the appropriate digital test capability.

Boundary scan tests are ideally suited to be run on an ICT system, but again the correct digital resources are required. Even complex functional test can be performed if the test system has a synchronized analog and digital subsystem. For that reason, if you are taking advantage of programming or using boundary scan, you don't need to use analog opens techniques on those devices.

**Why Not Use Digital Testing?**

The two main problems that have stopped the continued use of digital in-circuit techniques when access is available have been the lack of digital vector models and the inadequate capabilities of some digital ICT systems.

**Digital Models**

Many companies and test program suppliers still provide test vector de-

vice model programming services. Some are on the back of model development for component test, but most are related to the use of JTAG within the device design.

Most large devices and programmable devices have boundary scan to either test or program the device. With tools such as Teradyne's BasicScan, it is easy to automatically generate a digital model quickly from the BSDL, and it can even deal with configurations and tied pins. Other simple devices such as buffers, latches, and memory devices can be modeled, but manufacturers sometimes still use analog opens techniques because it is an easy development option.

**What Is Required to Provide Digital Vectors?**

To test the latest generation of digital components, the tester pin electronics must have certain characteristics. Today's lower voltage devices are based around 1-V logic which is very different from the 5-V and 3.3-V logic of the

1980s (Figure 2). Most boards still have some traditional logic families so the tester needs to deal with voltages from -2.5 V to 5.5 V but use the programming resolution to test 0.8-V logic with its 240-mV windows for both drive and sense (Figure 3).

Generally, measurement and test systems need to be 10 times more accurate than the UUT; in this case, better than 24-mV drive/sense accuracy. Dual-level logic thresholds for input and output also are required to guarantee accurate high- and low-level levels (Figure 3). And to perform whatever function is required for test, the digital pins must be able to drive, sense, tristate, or act as pull-up/down resources for the net in case these are not on the UUT but on another board or backplane. All these features need to be programmable on a pin-by-pin basis; otherwise it becomes very difficult to build fixtures to accommodate the different requirements of each logic family.

The complexity of modern devices means that a number of vectors need to be applied. Timing errors between signals must be <5 ns across the pin fields, which could be thousands of channels. When the signals are applied, they need consistent and repeatable timing that only a dedicated digital controller can ensure.

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The reason for lower voltages is the reduction in power needed in modern electronics and the small die sizes used in device manufacturing. This means that during digital testing the amount of energy needs to be controlled to avoid damaging any of the devices. Not only do you need to limit current, but also the time spent forcing logic values must be controlled.

Some devices require 600 mA to force a low logic level to a high, and others would be damaged if 100 mA were used. Some devices can take several milliseconds of backdriving while others should be limited to microseconds. Consequently, the test system needs to be able to measure and control backdrive current and time characteristics on the fly in real time (Figure 3).

If the test system does not have these features, then it may be easier and more prudent to use analog opens techniques than risk damaging the UUT.

## Conclusion

Analog opens has a place within the ICT system suite of test techniques. It is ideal for testing connectors, sockets, and devices that cannot be tested with digital vector models. However, manufacturers can use high-performance ICT systems to perform digital vector testing and gain the benefits of faster test throughput, lower cost fixtures, more reliable test measurements, and higher fault coverage.

## About the Authors

*Alan Albee, the in-circuit test product manager working in Teradyne's System Test Group, has worked at GenRad and Teradyne for 28 years in various engineering, applications, product support, and marketing positions. He has authored numerous technical articles on topics related to board test and has been awarded two patents. Mr. Albee has a B.S. in industrial science from Fitchburg State*

*College. Teradyne, 700 Riverpark Dr., MS-NR-7001-1, North Reading, MA 01864, 978-370-6238, alan.albee@teradyne.com*

*Michael J. Smith has more than 30 years experience in the automatic test and inspection equipment industry with Marconi, GenRad, and Teradyne. The author of numerous papers and articles also has chaired iNEMI's Test and Inspection Roadmapping Group for many years. Mr. Smith has a BSc(Hons) in control engineering from Leicester University and is a member of the Institution of Engineering and Technology (MIET). smithmj@btinternet.com*

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