

## Management of DPMO Metrics Reduces the Cost of PCB Assembly

Amit Verma  
Teradyne Inc.  
12365 First American Way, San Diego, CA  
[amit.verma@teradyne.com](mailto:amit.verma@teradyne.com)

### ABSTRACT

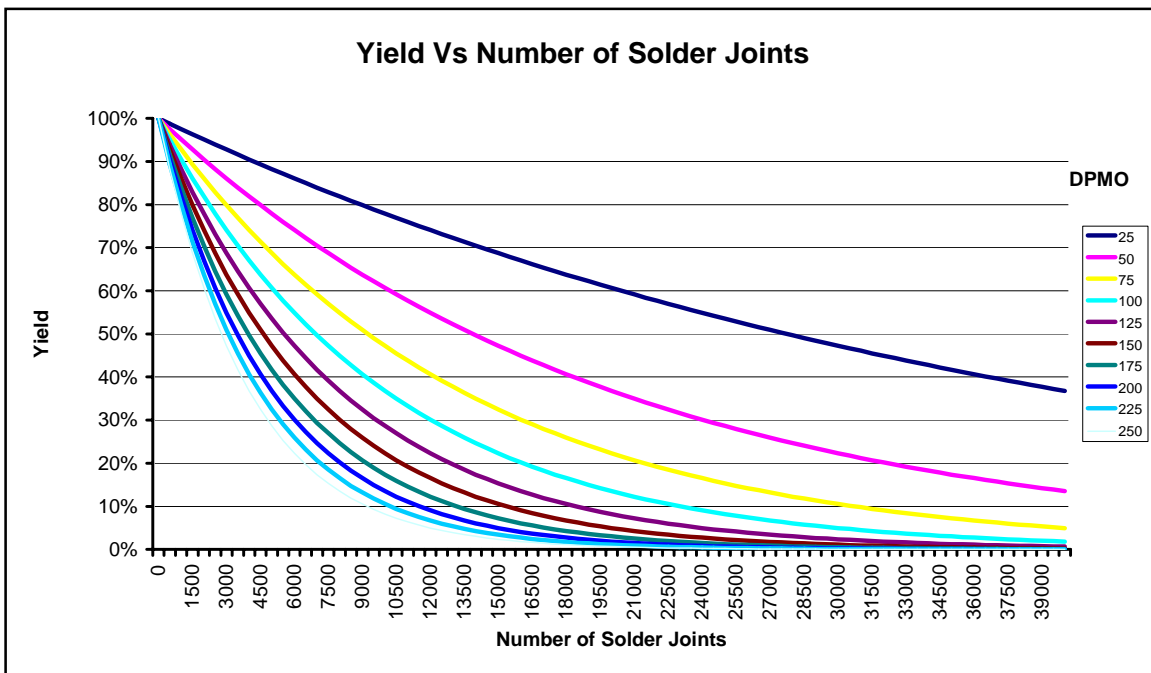
Manufacturers can use DPMO metrics to reduce the cost of PCB assembly with fewer resources. DPMO data can be used for predicting the fault spectrum on future products, quoting new business, setting quality targets for manufacturing, defining test strategies, predicting yields, or estimating shipped quality levels. Manufacturers can input DPMO and BOM data into cost calculator tools to estimate manufacturing costs. When combined with a few site-specific assumptions about labor rates and test strategy, roughly 80% of PCB assembly costs fall into place once there is a clear definition of the DPMO. In this way, manufacturers can determine targets for both in-process quality and financial profit and loss. Tools are now available to the industry that make use of DPMO data for strategic decision making applications. Use case examples are shown.

Keywords: Quality, DPMO, Defects, Yield, Cost, DFM, DFT, EMS, Business, AXI, X-ray, AOI, and SPC

### INTRODUCTION

The electronics manufacturing industry's conversion cost roadmap<sup>1</sup> requires a reduction in the cost per IO of each assembly over time. An important factor in reducing this conversion cost is enabling higher quality, thereby delivering higher utilization, shorter product cycle times, reduced cost of test, inspection, repair and scrap and lower manufacturing costs overall.

If manufacturers are not able to improve their quality performance, they will not be able to reduce their manufacturing costs. Faced with the increasing complexity of electronics assemblies, manufactures face the dilemma of declining yield, increased cost of test and inspection, lower line utilization, higher levels of scrap and rework and longer product cycle times (see figure 1).



**Figure 1** Yield declines as the number of solder joints per board increases. To use the chart, determine product DPMO rate and then estimate yields using the appropriate curve. Equation 2 is used to calculate yield (see below).

Defects per Million Opportunities (DPMO) is the preferred metric to enable improved quality performance. An effective management process around DPMO metrics can deliver the following benefits to electronics manufacturing businesses:

- creating an environment where the delivered quality of manufacturing processes is continually improved
- creating a process to better define operational improvement plans for manufacturing sites relative to competitors and industry norms
- enabling accurate estimates of PCB assembly cost early in the product life-cycle for quoting new business
- creating actionable DFM and DFT processes
- reducing costs of assembly, test, rework and scrap
- improving line utilization
- allowing manufacturers to better prioritize the deployment of constrained resources in a global environment

### DEFINITION OF DPMO

An good source for a detailed definition of DPMO is “*IPC Standard 9261: In-Process DPMO and Estimated Yield for PWAs*”.

At a generic level, DPMO is simply “*the number of defects measured in a population*” **divided by** “*the number of opportunities for the defect to have occurred in the same sample*”.

$$DPMO = \frac{\text{number\_of\_defects}}{\text{number\_of\_opportunities}} \times 10^6$$

### Equation 1

Many in the industry measure DPMO independently for terminations vs. components vs. overall DPMO.

A termination DPMO would be denoted as “DPMO<sub>t</sub>”, and component DPMO as “DPMO<sub>c</sub>”, for example. Each type of DPMO would have a unique set of defect types that are included in *number\_of\_defects*. *Number\_of\_opportunities* will also vary by type.

Termination DPMO<sub>t</sub> might include shorts, opens and solder quality problems in *number\_of\_defects* while *number\_of\_opportunities* would be the number of terminations on the board.

Component DPMO<sub>c</sub> might include missing component, non-functioning component, wrong component and skewed component in *number\_of\_defects* while *number\_of\_opportunities* would be the number of components on the board.

The overall DPMO would include all defect types and all opportunities measured throughout the manufacturing process. When multiple test stages are used, the individual DPMO measured at each step can be summed to determine the overall DPMO. Relevant details can be found in the IPC 9261 standard.

### WHY IS YIELD LOSING FAVOR TO DPMO AS THE PREFERRED QUALITY METRIC?

The 1<sup>st</sup> pass measured yield at a test stage like in-circuit test (ICT) has been used for many years as the benchmark quality metric. Modern test strategies that combine multiple techniques including automated optical inspection (AOI), automated x-ray inspection (AXI), and ICT to provide full test coverage are rendering the ICT measured yield metric less useful.

The issue is not simply that multiple test steps mandate that multiple yields be monitored – hence making the administration effort more cumbersome. More importantly, it is the validity, precision and unambiguous meaning of the measured yield metric that is being compromised in today’s test environment.

The “measured yield” at a given test stage is intimately linked with the “test coverage” provided by the stage. In previous years, ICT provided excellent test coverage on PCBs because bed of nails access to the board was assured; access was upwards of 90% and even 100% in many cases. The types of defects that manufacturers wanted to find in “days gone by” were also detectable by ICT. In today’s test environment however, bed of nails access is not assured; access can vary anywhere between 0% and 100%. Furthermore, AOI and AXI are increasingly used to find structural defects like insufficient solder or missing bypass capacitors that cannot be found by ICT means. The result is that ICT coverage is often much lower than it was previously, which compromises the utility of the ICT yield metric (see figure 2).

In addition, manufacturers are more often implementing distributed test strategies with multiple test machines; therefore they often intentionally reduce the test coverage at one machine, knowing instead that another test step provides the required coverage. This approach reduces test overlap and is often used as a means to achieve objectives like reduced test time, reduced capital expenditure and reduced ICT fixture cost. Another complication is that distributed test strategies often place equipment at points in the line that provide quick feedback to the previous assembly step. Because many test steps are used, each at a different location in the process flow (post place, post reflow, post wave etc.) the coverage

Yield	Test Coverage	Defects Found (per board)	Total Defects Present (per board)
22%	75%	1.5	2
37%	50%	1	2
61%	25%	0.5	2
78%	13%	0.25	2
91%	5%	0.09	2

**Figure 2** The defects present at time of test is unchanged for all cases. Notice the yield increases as the test coverage declines (Equation 2 is used to calculate yield). The table shows why the yield metric is compromised when test coverage declines and coverage is inconsistent from test step to test step: the yield “artificially” increases above 90% by reducing the test coverage.

of each test can be different depending on which components have already been populated at time of test. Gone are the days when all products were tested at ICT at the same stage of assembly with about the same ICT coverage.

All these factors, combined with product-to-product variability, lead to a situation where the test coverage on product ‘A’ at test step ‘X’ (where X could be ICT or AOI or AXI) can be radically different than the test coverage on product ‘B’ at the same stage - hence a comparison of the yield between product ‘A’ and product ‘B’ has little meaning or credibility. More and more often, the measured yield metric is only valid within the frame of reference of the product where the yield was measured – not from one product to another.

Furthermore, an arbitrary assessment that the ICT yield should be greater than “90%” also lacks credibility. As shown by Figure 2 above, if the coverage is reduced enough at ICT, the yield can “artificially” increase above 90% regardless of any improvement or change in the actual quality of the product.

Also complicating matters is the fact that defects have often been detected and repaired before boards even reach ICT in a distributed test strategy. Therefore the use of ICT measured yield as an assessment of overall process quality does not account for the defects that have already been removed; note that these previously found defects might even outnumber the defects found at ICT!

The advantage of the DPMO metric over measured yield is that DPMO measured at each test step can be easily summed to provide an overall DPMO rate. This overall DPMO more accurately represents

product quality regardless of where the defect was found in a distributed test strategy.

For these reasons, the use of a measured yield metric to assess manufacturing quality is losing favor relative to the DPMO metric that has more validity when comparing product ‘A’ to product ‘B’ regardless of process flow or differences in test coverage due to distributed test strategies and loss of ICT access. The industry is increasingly adopting the DPMO metric as a more absolute measure of quality that allows comparisons relative to target values on other products, industry “best of breed” targets and comparisons between different manufacturers.

### LIMITATIONS OF DPMO AS A QUALITY BENCHMARK

Although the overall DPMO rate provides a much better mechanism (than measured yield) for quality comparisons between products (and from products to industry benchmarks) as described above, its limitations should also be understood.

DPMO is susceptible to problems of poor test coverage. Regardless of where defects are found in a distributed test strategy, if a defect simply is not detected anywhere in the process, it can never be included in a DPMO calculation. Therefore, the overall DPMO rate can only reflect a valid overall DPMO if the total test coverage of all test steps summed together is complete. Whereas confidence is lost in “yield” when any single test step lacks coverage, the overall DPMO rate is only weakened when all steps summed together lack the necessary coverage.

A factor to consider when comparing DPMO rates between products is their relative “complexity” or “manufacturability index”. Although the comparison of DPMO between a high-volume automotive PCBA with a total of 3000 joints to a telecommunications board with 30,000 joints might be technically valid; its practicality may be limited since the possibility of achieving similar levels of quality between the products is remote. When comparing DPMO between products and to benchmarks, it is important to consider what factors might identify valid “peers”; complexity indices are useful in this regard.

### PREDICT YIELD WITH DPMO

Note that PCB yield can be estimated from the number of defects that are predicted from DPMO using the following equation:

$$Yield = e^{-(number\_of\_defects)} \times 100\%$$

**Equation 2** Note that the “number\_of\_defects” is calculated from Equation 1 using DPMO.

The prediction of yield using DPMO data is a significant benefit and is discussed in more detail later in this paper. When predicting yield at any specific test stage, only those defects that will be found by the test stage should be included in the DPMO rate.

Although the equation provides a good estimation of the board yield in most cases; it is less accurate in some types of manufacturing processes due to the clustering or grouping of defects at a single device location<sup>2</sup>. For most PCBs however, the Poisson statistical distribution (as provided by the above equation) is a good approximation to PCB yield.

### **IMPLEMENTATION OF DPMO IN THE MANUFACTURING ENVIRONMENT**

It is significantly more difficult to measure DPMO than the traditionally used "yield". Whereas yield is often automatically computed by most factory data collection systems or even reported within the GUI interface of many test machines, few manufacturers today have the means to automatically compute DPMO.

While the *number\_of\_defects* is readily available, the *number\_of\_opportunities* is often not calculated by most test machines or factory information systems (FIS). Although the information required to compute the *number\_of\_opportunities* is always embedded within the bill of material (BOM) or the "list of devices tested by the inspection system", most manufacturers' software does not explicitly compute the figure. As more companies migrate to the use of enterprise databases, the implementation of DPMO becomes easier.

Not surprisingly, some leading manufacturers have already enabled the calculation of DPMO within their factory information systems. The most basic implementations compute both the DPMO at each test stage in the process flow and the overall DPMO. More sophisticated solutions would allow computations of DPMO for specific subgroups as well. Examples of these sub-groups are package type (PBGA, RPAK, 0805 chips or .5mm QFP etc.) or even part number.

DPMO by package type enables a wide variety of highly effective root cause problem solving methods. As reported by Flextronics, the use package type data within the context of a continuous improvement plan helped reduce defect rates by 83% (from 635 DPMO to 93 DPMO) on a single product over 3 months<sup>3</sup>. The reporting of this information can make it apparent, for example, that a QFP256 on product 'A' has double the DPMO rate of the same package on product 'B'. The quality improvement team can

quickly focus their efforts on the out-of-control sub-groups that are causing the highest impact or drag on profitability. Without package type data reporting, the high QFP256 defect rate might be hidden by an aggregate quality statistic representing a larger number of sub-groups. The specificity of package type DPMO reporting isolates valid sub-groups for easy identification of out-of-control situations.

DPMO enables more "action-able" quality information on the manufacturing floor. Individuals can focus their efforts on the "vital few tasks" and take more immediate corrective actions with fewer resources.

"DPMO by part number" is another highly actionable metric. For example, an EMS company could identify that different suppliers of the same SOIC16 chips were yielding vastly different DPMO rates. The root cause could be a supplier issue (incoming bent leads, co-planarity or even solder wetting) or a handling issue in the EMS' own receiving area. The bottom-line is that DPMO data helps save time, money and reduce scrap.

### **DPMO TAKES THE MYSTERY OUT OF BOARD ASSEMBLY TO DELIVER STRATEGIC VALUE**

Perhaps the most valuable use of package type and part number DPMO data is their use in predicting the number of defects that will occur on future products. The bill of material combined with DPMO can be used to compute the fault spectrum for any PCBA. This data may be used for quoting new business, setting quality targets for manufacturing, creating more action-able DFM processes, defining test strategies, predicting yields, and estimating shipped quality levels – all before a single board is ever manufactured. Examples of these use cases are shown later in the paper – see below.

To a good degree, once there is a clear definition of the BOM and the defects that will occur during manufacturing, 80% of PCB assembly costs fall into place given a set of site-specific assumptions about labor rates and test strategy. For this reason, it is easy to understand why DPMO data is of strategic and competitive value to electronics manufacturers.

A global electronics manufacturer may use reported DPMO rates to determine which factories have the best quality performance. In addition, they could input DPMO and BOM data into cost calculator tools to estimate manufacturing costs and award new business. In this way, they can determine targets for both in-process quality and financial profit and loss - a check-and-balance for some of the most critical elements of the business.

## **INDUSTRY DPMO BENCHMARKS PROVIDE COMPETITIVE INSIGHT**

Because manufacturers can use DPMO information to help allocate new business and define operational improvement plans, one can understand why they have a desire to understand their own DPMO performance relative to others or an industry “best of breed” benchmark.

There are currently two groups of manufacturers working to share DPMO rates so that relative standing can be determined. The data collection methodology used by the teams assures anonymity of the participants’ data and allows each manufacturer to share their DPMO without fear of competitive disadvantage. The “SMART Group” in the United Kingdom is running the “PPM Project”; the other team is the “National Electronics Manufacturing Initiative (NEMI) DPMO Project”. Upon the conclusion of these projects, a limited amount of information will likely be made available to the industry – the primary beneficiaries are the project participants themselves.

Both projects are “industry firsts” and demonstrate a consensus and confidence amongst manufacturers in the strategic value of DPMO metrics.

## **INDUSTRY TOOLS SUPPORT USERS OF DPMO METRICS**

Given manufacturers are investing time and resources in measuring DPMO rates for their assembly processes, what tools are available to them to leverage the information collected for cost reduction activities and strategic decision making?

Some EMS companies have created their own proprietary tools that use DPMO data to help perform DFM activities, set quality targets and define test strategies - one example is the Quality Modeling System (QMS) reported by Celestica<sup>4</sup>. The QMS was perhaps the first tool of its kind to use DPMO information for a comprehensive set of quoting, and target setting activities.

More recently, manufacturers have come together within consortiums like NEMI to create cost modeling tools that make use of DPMO data. The “NEMI Test Strategy Project”, which has 10 member companies, has developed a spreadsheet based cost model from the best practices from each of the participants. The test strategy cost model is available free-of-charge to the rest of the industry at the footnoted web address<sup>5</sup>.

More feature-filled ‘off-the-shelf’ commercial tools are also available to the industry. Teradyne’s

“Strategist”<sup>6</sup> software allows users to predict the defects that will occur based upon a bill of material and DPMO (default DPMO data is available for users that may not have their own statistics). Because the tool uses CAD as well as ICT device libraries, it can accurately determine ICT, AXI and AOI access constraints and test coverages. The user can optimize their test strategy based upon the predicted fault spectrum (calculated from DPMO) and thereby estimate yields, costs and shipped quality levels well before a single board is ever manufactured.

As more manufacturers migrate to the use of DPMO as their preferred quality metric, more commercial software tools will become available to help with the strategic decision making applications described.

## **DPMO USE CASE EXAMPLES FOR STRATEGIC DECISION MAKING**

The use cases below are typical examples of how DPMO data is used to aid in strategic decision making for PCB assembly. All examples employ functionality resident in Teradyne’s “Strategist”<sup>6</sup> software.

### **Create libraries to manage site specific DPMO**

Users can create libraries of DPMO by package type (see figure 3). Both joint and component level DPMO can be stored in a library. Different libraries can manage information for different manufacturing sites or for products with different levels of complexity – users can select the appropriate library based on product objectives. If users do not have libraries, defaults are pre-populated for rapid assignment of both joint level and component level DPMO (see figure 4). The accuracy of computed defect or yield statistics should be viewed as a “reasonable” or “best available” estimate – the computed data is only as accurate as the incoming DPMO used; assumptions should be refined on sequential iterations.

### **Predict the defect spectrum for future products**

Historic DPMO rates can be used to predict the fault spectrum for future products manufactured (see figure 5). Fault spectrum data is useful for determining what type of test strategy is optimal and which components require more comprehensive test coverage. This data is also useful to predict costs of repair and scrap.

### **Plan test strategies, determine fault coverage and estimate shipped quality levels**<sup>7</sup>

Engineers can design optimized test plans by modeling the fault coverage of each individual test stage on a component and pin level based upon DPMO data. Engineers can determine which ICT test points

The screenshot shows the 'Data Editor' window with a 'Part Library' tab selected. It displays a table with columns for Package, Pins, Package DPMO Top, Package DPMO Bottom, Package Joint DPMO Top, Package Joint DPMO Bottom, and Used By Components. A progress bar at the bottom indicates 'Invalid (41)' at 100% and 'Valid (0)'.

Package	Pins	Package DPMO Top	Package DPMO Bottom	Package Joint DPMO Top	Package Joint DPMO Bottom	Used By Components
1 CC7257P	2	500	500	100	100	C47, C48, C9, C51, ...
2 CC2225	2	50	50	50	10	C44, C45, C1, C27, ...
3 CC1812	2	50	50	50	10	C8, C29
4 SO200-4	4	50	50	50	10	Y1
5 PLC50-20B	20	50	50	50	10	U12
6 SOT23B	3	50	50	50	10	CR8
7 PRBPOINT40B	1	Undefined	Undefined	Undefined	Undefined	TP152, TP156, TP1...
8 PLC50-28KB	28	50	50	50	10	U8
9 700C20-4	4	50	50	50	10	R42
10 SO50-28AN	28	50	50	50	10	U14, U15
11 SO50-15B	16	Undefined	Undefined	Undefined	Undefined	Z4, Z1, Z2, Z3
12 D100-4AFET	4	Undefined	Undefined	Undefined	Undefined	Q6, Q4, Q5
13 SOT23E	3	Undefined	Undefined	Undefined	Undefined	CR1
14 SO50-20AN	20	Undefined	Undefined	Undefined	Undefined	U10, U13
15 INDUCTOR	4	Undefined	Undefined	Undefined	Undefined	T2, T1
16 SOT23-FET1	3	Undefined	Undefined	Undefined	Undefined	Q2
17 600C21C	2	Undefined	Undefined	Undefined	Undefined	CR4
18 S100-3A	3	Undefined	Undefined	Undefined	Undefined	WT69, WT66, WT6...
19 SO50-14AN	14	Undefined	Undefined	Undefined	Undefined	U3, U16, U6
20 S100-2A	2	Undefined	Undefined	Undefined	Undefined	WT24, WT12, WT1...
21 PLC50-52KB	52	Undefined	Undefined	Undefined	Undefined	U4

**Figure 3** Users can create libraries of DPMO by package type to predict the defect spectrum for products more accurately. Libraries can be created for different product types or manufacturing sites.

The screenshot shows the 'GR Force/Strategist - [BOARD - \_PAD5]' window. It features a 'Setup' tab and a 'Current Model Library' section with a file path 'C:\Apex\_ISM\apex\_ism.mdb'. The 'Default DPMO Settings' table is as follows:

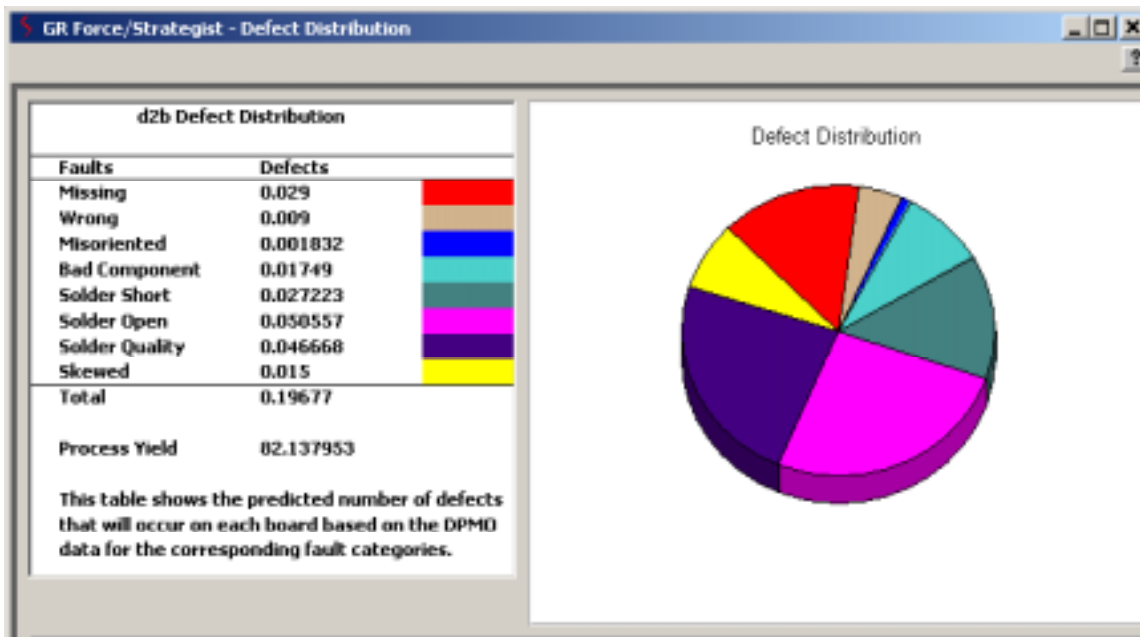
Setting	Value
Package Top	75.00
Package Bottom	75.00
Joint Top	32.00
Joint Bottom	32.00

Below this is a 'Faults' table with columns for Fault Type, Category, and DPMO Allocation %:

Fault Type	Category	DPMO Allocation %
Missing	Component Fault	38.0
Wrong	Component Fault	12.0
Misoriented	Component Fault	5.0
Skewed	Component Fault	20.0
Function	Electrical Fault	20.0
Value	Electrical Fault	5.0
Solder Short	Solder Fault	22.0
Solder Open	Solder Fault	42.0
Solder Quality	Solder Fault	36.0

At the bottom, there is a 'Fault Description' field, a 'Data Warnings/Errors' checkbox, and a 'Load Board Data' button.

**Figure 4** If libraries are not available, default DPMO values can be rapidly assigned.



**Figure 5** The defect spectrum for a product can be estimated using DPMO data. This data can help to determine what type of test strategy should be used.

maximize coverage on the computed fault spectrum while concurrently taking into account the complementary coverage of other test steps like AOI or AXI. Because DPMO reflects the relative probability of defects to occur on specific components and joints, access can be removed on the locations least likely to produce defects. The software uses ICT device libraries and allows engineers to make access tradeoffs prior to layout routing, so that board designers can place test pads where they are most required. In access constrained environments, this methodology results in intelligent removal of access and highest test coverage.

The software computes the defects present at each component and joint location on the board. When combined with the test strategy, the coverage of each test stage can be computed (AOI, AXI, ICT, and FPT). The number of defects found by each test step and those defects NOT found are also known. In this way, the shipped quality level provided by the test strategy can be determined. The shipped quality level is useful to compare the effectiveness of different test strategies at meeting the reliability requirements of the product's end use environment (see figure 6).

Engineers can determine, for example, that test strategy 'A' can cost double the capital expense and double the cycle time of strategy 'B', while only providing 10% higher shipped quality. For business reasons, strategy B may be preferred. This information can be particularly valuable to EMS and OEM teams as they try to achieve consensus on a test strategy that provides the necessary fault coverage at the targeted throughput and cost objectives.

#### **Determine quality targets for production ramp**

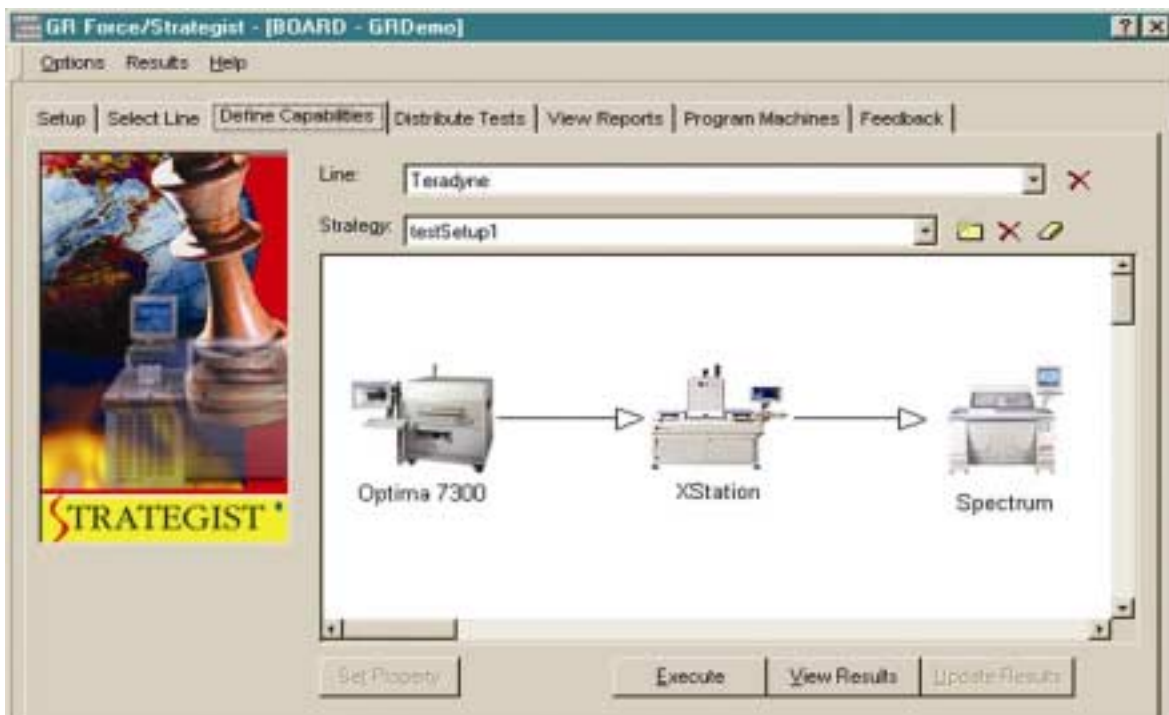
Factory DPMO targets or industry benchmarks can be saved in a DPMO library and used when modeling a specific PCB. Because the test coverage and defects found at each test step are known, the software can estimate the yield at each stage. These yield targets can be used during production ramp. Gaps between target values and actuals can indicate out of tolerance defect rates that require attention by production quality teams (see figure 7).

#### **Provide cost-justified DFX feedback**

A common problem experienced by process engineers in conducting DFX activities is that the cost of a recommended design change is difficult to quantify. This problem is often amplified by the organizational separation that often exists between OEM designers and EMS DFX engineers. Using this software however, engineers can quantify the impact of a specific design violation and its impact on the entire manufacturing process. The user can alter the DPMO assumptions on specific components (and their joints) to show how product quality would be worsened (or improved) by a specific design change and thereby quantify the impact on yield, repair costs, scrap and shipped quality levels. This creates a more actionable DFX cycle.

#### **Create quotations for winning new PCB assembly business more quickly and more accurately**

The defect spectrum, test strategy, yield, and shipped quality level can be easily computed within the software when CAD information for a specific PCB is provided.



**Figure 6** The user can plan different test strategies to determine which equipment set delivers the required fault coverage and shipped quality level at the targeted throughput and cost objectives.

Predicted Total Defects per board	Process Yield	Item	GR XStation		GR TestStation		Escapes per Board	Final Yield	% Defective	Line Effectiveness
			Predicted	Actual	Predicted	Actual				
0.080871	92.23%	Defects per board Detected	0.073289	NA	0.007127	NA	0.000455	99.95%	0.05%	99.44%
		Yield	92.93%	NA	99.29%	NA				
		% Defective	7.07%	NA	0.71%	NA				
		Machine Effectiveness	90.62%	NA	8.81%	NA				

**Figure 7.** Users can estimate test yield from the DPMO, fault spectrum and test coverage of each machine can be used to set targets during production ramp.

When combined with a few site-specific assumptions about labor rates and test strategy, roughly 80% of PCB assembly costs fall into place. In this way, manufacturers can perform quotations more accurately and more quickly with fewer resources.

## CONCLUSION

Manufacturers can use DPMO metrics to reduce the cost of PCB assembly with fewer resources. DPMO provides more action-able quality information on the production floor. The bill of material (BOM) combined with DPMO can be used to compute the fault spectrum for future products. This data may be used for quoting new business, setting quality targets for production ramp, defining test strategies,

predicting yields, or estimating shipped quality levels – all before a single board is ever manufactured.

Manufacturers can input DPMO data into cost calculator tools to estimate manufacturing costs. When combined with a few site-specific assumptions about labor rates and test strategy, roughly 80% of PCB assembly costs fall into place once there is a clear definition of DPMO and BOM. In this way, manufacturers can determine targets for both in-process quality and financial profit and loss - a check-and-balance for some of the most critical elements of the business.

The industry is working cooperatively on DPMO projects – this demonstrates confidence in the value

of DPMO metrics. Tools are available to the industry that make use of DPMO data for strategic decision making applications. Use case examples were shown – manufacturers can apply the demonstrated methods to their own business processes.

## GLOSSARY

9261	IPC standard 9261: In-Process DPMO and Estimated Yield for PWAs
AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
BOM	Bill of Materials
DFM	Design for Manufacturability
DFT	Design for Testability
DFx	Design for manufacturability and testability
DPMO	Defects per Million Opportunities
EMS	Electronics Manufacturing Services
FIS	Factory Information System
FPT	Flying Probe Test
FT	Functional Test
ICT	In-circuit Test
IO	Component Input/Output termination (pin)
MVI	Manual Visual Inspection
NEMI	National Electronics Manufacturing Initiative
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PBGA	Plastic Ball Grid Array
PWA	Printed Wiring Assembly
RPAK	Resistor Pack
QFP	Quad Flat Pack

## ABOUT THE AUTHOR

Mr. Verma is the chair of the National Electronics Manufacturing Initiative (NEMI) “Test Strategy” project and participates in the “DPMO” project; both projects have broad participation from leading professionals in the electronics manufacturing industry. Mr. Verma also chairs the IPC “7-32 Automatic Inspection Technologies Subcommittee”. Amit has written numerous papers on test strategies, process control and imaging technology for APEX, Etronix and Nepcon conferences; as well as articles for various trade magazines.

Mr. Verma has over 7 years of experience designing distributed test strategies for complex PCB Assemblies. Prior to joining Teradyne, Mr. Verma was a Staff Engineer at a major EMS provider where he played a major role defining test strategies and purchasing ATE hardware.

---

## REFERENCES

- <sup>1</sup> See NEMI 2000 Roadmap, Board Assembly Technologies, Table 2: Conversion Costs
- <sup>2</sup> For more information on clustering of defects and its impact on the estimation of board yield, see “Defects, Fault Coverage, Yield and Cost, in Board

---

Manufacturing” written by Mick Tegethoff, published in the proceedings of the 1994 International Test Conference.

<sup>3</sup> “AXI: SMT Process Improvement Tool”, Feng, Djaja & Rocha. Proceedings of the SMTA International Conference, Chicago 2002.

<sup>4</sup> “Complementary Test Strategies on High Complexity Boards” by Verma, Ogden & Kokoska. Circuits Assembly August 2000 p.28.

<sup>5</sup>[http://www.nemi.org/projects/ba/test\\_strat.html](http://www.nemi.org/projects/ba/test_strat.html)

<sup>6</sup> Strategist is a commercially available software tool manufactured by Teradyne. A web seminar can be viewed at the following URL “Designing Test Strategies for Modern PCB Assembly”. [http://www.teradyne.com/prods/cbt/products/library/general\\_lib.html](http://www.teradyne.com/prods/cbt/products/library/general_lib.html)

<sup>7</sup> “Optimizing Test Strategies for Modern PCBAs with Limited ICT Access”, Robinson & Verma. APEX 2002 Conference Proceedings.