Backdrive Current-Sensing Techniques Provide ICT Benefits

by Alan Albee, Teradyne

In-circuit testers rely on bed-of-nails-type fixtures that give the tester access to every node (or net) of the printed circuit board (PCB). Using this access, the tester takes a divide-and-conquer approach, testing each component as if it were the only component on the assembled PCB.

If all the individual components pass the tests, then it is likely that the board is free of assembly faults and will function correctly in its target application. This test strategy is possible because the tester uses techniques that isolate the component being tested from the unwanted electrical effects of the components that surround it.

Backdriving has been part of in-circuit testing for more than 20 years, but always the subject of controversy. A new pin technology could put an end to the debate.

An Overview of Digital Isolation Techniques

Figure 1 shows an example of a digital circuit. When component U8 is the device under test (DUT), the tester applies a series of digital test vectors to the input pins of U8 and measures the output pin to make sure it responds as expected.

To ensure that the tester can drive the input pins of U8 to the required logic states, the digital pin drivers are designed as low-impedance current sources that typically can source or sink 600 mA or more of current. This current source momentarily forces nodes on the board to the logic levels required by the test. This technique of temporarily overdriving component outputs to force a node to its opposite logic state commonly is referred to as backdriving.

Referring to Figure 1, if N1 or N2 is a logic low, then the output of U3 will drive node N8 low. If, during the test for U8, the tester is told to drive pin 4 high, then the driver attached to node N8 temporarily sources enough current to backdrive the output of U3 so a logic high voltage is achieved on U8 pin 4.

Teradyne's GR TestStation family of in-circuit testers with UltraPin digital pin electronics offers backdrive current sensing and programmable backdrive control features, 40-mV driver/sensor pin accuracy for testing low-voltage technologies, and a paired driver/sensor pin architecture that performs automatic driver verification.

Disables

To avoid bus conflicts and minimize backdriving, in-circuit testers use a technique called Disables. In Figure 1, the U5 output can be controlled by an output enable signal. Driving node N9 to a logic low value forces the U5 output to a high-impedance state, effectively shutting it off so that it does not conflict with the U8 pin 16 output.

Disables also are effective at eliminating the need to backdrive outputs when driving component input pins. Referring again to the example circuit, the U1 output can be controlled by an enable signal. Driving node N6 to a high logic state places the U1 output in a high-impedance condition that effectively removes it from the circuit. By disabling U1, the tester driver attached to node N7 no longer needs to use any backdrive current when it applies test vectors that drive U8 pin 11.

This Disable technique only is possible on component outputs designed with tri-state logic. Two-state component outputs, like the outputs of U2 and U3 in Figure 1, cannot be shut off—they are designed to always be in one of two states, either high or low.

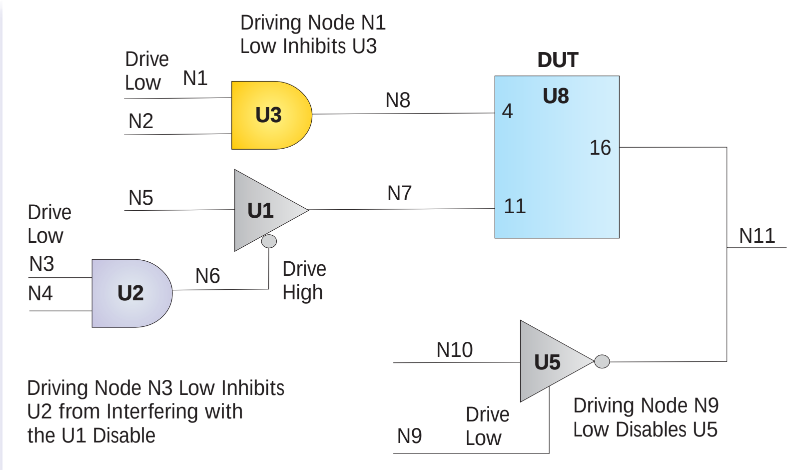

Figure 1. Example of a Digital Circuit

Inhibits

In Figure 1, if nodes N1 and N2 are high, then node N8 will be driven to a logic high value by the output of U3. During the U8 test, any test vectors that call for N8 to be driven low will cause the tester driver to supply a large amount of current to temporarily force node N8 low.

If the logic state at either nodes N1 or N2 changes from a high to a low, then the U3 output would transition from a logic high to a logic low. If this occurs while the output is being backdriven, then the energy that was being used to backdrive the output no longer is needed and dissipates as a transient voltage spike on the backdriven node.

A transient voltage spike can damage components on the node when its magnitude is large enough to violate the published maximum or minimum voltage specifications. More likely, however, the transient voltage will cause the test to fail because it will appear as a brief logic state transition to the component being tested.

To prevent this from happening, in-circuit testers use a technique called Inhibits. In Figure 1, the output from U3 is prevented from changing during the U8 test by driving node N1 low. This keeps the U3 output low and inhibits it from changing while U8 is being tested.

By analyzing the circuit interconnections and using Disable and Inhibit techniques at multiple levels, the tester isolates the component under test and significantly quiets the board circuitry so that high-integrity signals can be applied. These isolation techniques make in-circuit digital testing accurate, stable, and repeatable so that false failures do not occur during production testing.

Can Backdriving Be Harmful?

Backdriving has been part of in-circuit testing for more than 20 years, but it always has been the subject of some controversy because it usually results in current flows that exceed component ratings. According to several industry studies, the misuse of backdrive techniques can unduly stress or cause permanent damage to digital components.[1]

Failures attributed to backdriving fall into two categories:

Thermal Failures

Current flowing through the backdriven component increases the temperature of the component's output junction and bondwires. The temperature increase depends on a number of variables including current level, duration, component packaging, and technology.

The temperature increase is magnified in the case of the common bondwire(s) of a component that has multiple output pins being simultaneously backdriven to the same logic state. In this case, the maximum safe backdrive time for an IC is a function of the number of outputs being driven and the sum of the currents.

The current flow caused by backdriving may cause failure in a bondwire if it raises its temperature above the melting point. Repeated current pulses, even though they do not raise the temperature of the bondwire above its melting point, may activate a fatigue mechanism in the bondwire that can cause latent defects and early-life component failures.

Transistor Latch-Up

Subjecting certain digital pins, primarily on CMOS technology components, to voltages more than a safe amount beyond the component supply voltages can force the transistors to enter a high-current, possibly self-destructive, latch-up state. The voltage overshoot and undershoot conditions that trigger the latch-up condition can occur during digital backdriving when an output that is being backdriven suddenly changes its logic state.

Preventing Backdrive Problems

To protect against the potentially damaging effects of backdriving, in-circuit testers use one or more of the following features:

Current Fold-Back

Some in-circuit drivers feature fixed-current fold-back circuitry to limit the amount of backdrive current that can be delivered by the driver over time.[2] This built-in hardware protection ensures that the bondwires on the backdriven IC do not have enough time to reach damaging temperature levels.

DEVICE LABEL: U182_B1:
DEVICE NAME: U182
DEVICE TYPE: 74FCT162501

PIN	NODE	NAIL	MAX. BACKDRIVE
1	PU0402	31	<= 50 mA
2	**XIOABLE**	**5015**	**158.12 mA**
3	XIOAB2	640	<= 50 mA
5	XIOAB3	671	<= 50 mA
6	XIOAB4	672	<= 50 mA
8	XIOAB5	648	<= 50 mA
9	XIOAB6	678	<= 50 mA
10	XIOAB7	3935	<= 50 mA
12	XIOAB8	655	<= 50 mA
13	XIOAB9	631	<= 50 mA
14	XIOAB10	656	<= 50 mA
21	**XIOBS0**	**4976**	**231.48 mA**
23	**XIOBS1**	**4979**	**218.69 mA**
24	**XIOBS2**	**4980**	**196.73 mA**
26	**XIOBS3**	**4986**	**261.91 mA**
27	PU0428	162	<= 50 mA
	XPRGMT	107	<= 50 mA
	PU0401	161	<= 50 mA
	OE4_2	**3061**	**540.80 mA**

During the test for U182, node OE4_2 and the drivers connected to pins 2, 21, 23, 24, and 26 required backdrive current. Test program developers can use this information to add isolation sections to the program that will eliminate backdriving on these nodes.

Figure 2. Example of a Backdrive Report

Test Time Limits

Some in-circuit testers have programmable timers that can control the maximum time a test will take to execute. This feature can be used as an additional safeguard to limit the duration of the backdrive time. By limiting the test execution time, the thermal stresses caused by backdriving are limited to the safe region of component operation.

Automatic Cool-Down Delays

Component pins can be unduly stressed not only from executing one test that is long, but also from a series of tests that drive the same node. For example, one component output pin may drive the input pins of 10 different components. That output will be backdriven during all 10 component tests. If these 10 components were tested sequentially, then the backdrive stress on that component could exceed component ratings.

To prevent outputs from being overstressed in these situations, some testers insert an automatic cool-down delay between each digital test. The delay factor ensures that the duty rate of the pin drivers will not exceed 10% (actively driving no more than 10% of the total test time).

Predictive Backdrive Analysis

Some in-circuit testers use predictive backdrive analysis software.[3] This software takes into account information from component models, circuit interconnections, and component technologies and then attempts to predict the backdrive current stresses that components will be exposed to during each test. Tests that exhibit backdrive stress levels greater than predefined thresholds are reported.

What Can Go Wrong?

These techniques, when used properly, eliminate the possibilities of stressing components due to backdriving. However, there are some situations that prevent the techniques from working effectively.

Faulty or Missing Disables

Due to the rapidly changing electronics market and the increased use of custom digital components, it is difficult for test-equipment vendors and test developers to keep their component libraries up to date with the latest models. Because of this, many test developers often are forced to use incomplete and unverified component models, or they may choose to use less thorough vectorless test techniques that do not require component models.

With incomplete or missing component models, the in-circuit software does not have all the information it needs to properly disable and inhibit surrounding components. Even when complete component model information is available, sometimes the circuit-wiring configuration prevents proper Disables and Inhibits from being generated. In these scenarios, it is possible to have tests without the proper isolation sections, resulting in excessive backdriving and possible transient voltage conditions on some component pins.

UUT Fault Conditions

The backdrive-protection features used by in-circuit testers work well when testing a fault-free PCB. However, a PCB being tested for the first time is likely to have defects. It is interesting to consider how PCB fault conditions can affect the backdrive-protection features.

Referring back to the example digital circuit, many fault conditions could cause abnormal backdrive conditions during the test for U8. Some examples include the following:

• An open on node N6 or an internal fault in U1 could cause the U1 output driver to always be enabled.
• A component with equivalent logic functionality, but different electrical characteristics, could accidentally be placed for U3.
• An internal fault in the output transistor for U2 could cause the output to drive more current than normal.
• A short to an unnailed node on the PCB may cause the tester driver to use more backdrive current than normal.

Traditional in-circuit testers typically do not detect these fault conditions. Instead, the drivers connected to the faulty nodes mask the fault by applying additional backdrive current to override the fault and achieve the desired programmed voltage. The test operator has no idea that more backdrive current than normal was needed to overcome these fault conditions.

Inaccurate Backdrive Predictions

Software that tries to predict backdrive currents assumes that all Disables and Inhibits are properly working and there are no faults on the PCB. It cannot accurately predict backdrive currents when those assumptions are wrong. Predictive backdrive analysis software also can be inaccurate simply due to normal component-to-component variations in device output current characteristics.

Backdrive Detection—A New Approach

A new generation of in-circuit pin technology makes it possible to measure and report actual backdrive currents and duration. This technology gives test-program developers new insight into the amount of backdrive current being used for each test and allows them to program backdrive current thresholds that detect additional faults during production testing.[4]

Backdrive Current Sensing

The new technology pin-driver circuitry includes current-sensing circuitry that indicates the magnitude of the backdrive current. This circuitry monitors, in real time, the amount of current the driver requires to achieve the programmed voltage on the PCB node that it is driving, as shown in **Figure 2**.

Programmable Backdrive Current/Time Limits

The new technology pin driver also is equipped with a timer that monitors the amount of time that the driver exceeds a specified backdrive current value. This enables the in-circuit tester to immediately react by shutting down backdriving on those nodes that exceed current and time thresholds.

Backdrive current thresholds can be set from 50 mA to 600 mA, and backdrive time limits can be set as low as 750 ns or as long as 23 ms. The resolution of the backdrive time-monitoring circuit makes it possible for the tester to detect backdrive conditions as short as one test vector.

The following example shows how a driver attached to PCB node N8 can be programmed to prevent backdrive currents greater than 150 mA from being applied for a duration longer than 750 ns.

ASSIGN LGC LVLA(N8) VIHA = 3.0 VILA = 0.2 BDIA = 150M BDIT = 750N

If the backdrive limits are exceeded during test execution, the tester stops the test and lists the tester drivers and PCB nodes that violated the programmed thresholds.

Benefits of the New Approach

Several benefits can be derived from the capabilities of this new technology pin driver:

- Accurate backdrive reporting for more reliable tests.
- Simpler test-program development by eliminating the need to run backdrive prediction software.
- Programmable backdrive thresholds for safer testing of sensitive component technologies.
- Increased fault detection by identifying backdrive currents that differ from the known-good board profile.
- Faster test throughput by eliminating the cool-down delays when they are not needed.

References

1. “Safe Operating Limits for Backdriving,” U.K. Ministry of Defence, Interim Defence Standard 00-53/1, Nov. 15, 1991.

2. Suto, A. J., “Controlled Overdriving With 228X Pin Systems,” GenRad.

3. “Safeguard In-Circuit,” Product Note 3065-2, Hewlett-Packard, 1985.

4. Patent Number: 6,114,848, “Direct Measurement Provision of Safe Backdrive Levels”, GenRad, Sept. 5, 2000.

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