

The Economics of In-Circuit Testing

Michael J. Smith

A methodology for examining the effect of ICT alternatives on the cost of verification, diagnosis and retest.

Even small improvements in defect coverage can have a surprisingly large impact on more expensive downstream verification and diagnosis, repair and retest operations, not to mention field failures and returns. It is important to consider the economic impact of such advancements when developing manufacturing test and inspection strategies. For example, in a scenario involving production of 150,000 boards per year worth \$40 each, a 5% improvement of in-circuit testing (ICT) coverage reduces total costs of test, repairs and returns by about 10%.

Here we present a methodology for examining

the effect of ICT alternatives on the cost of verification and diagnosis, repair, scrap, retest, and field failures and returns for a number of different products and manufacturing environments.

New chip packages and board assembly technologies are increasing component and pad densities to a level approaching 50 I/Os per cm², reducing electrical access to PCBs. Lower voltages also pose significant challenges to ICT because low voltage components are more difficult to test reliably and are more susceptible to damage from over-voltage and over-current test conditions. Higher functionality in electronics devices such as cell phones with built-in cameras and global positioning systems poses greater challenges for first-pass yield while reducing the diagnostic resolution of functional and system test.

Case study no. 1: Low volume assembler. These trends are having a negative impact on the defect coverage of ICT. Yet, ICT remains a critical element of nearly every assembler's test and

Table 1. Low Volume Asian Assembler's Costs of Debug/Diagnosis and Repair

Debug/Diagnosis and Repair Costs		ICT	FT	ESS	System
Hourly Labor Cost of Verification/Diagnosis	[\$]	\$2	\$2	\$2	\$2
Hourly Labor Cost of Repair	[\$]	\$2	\$2	\$2	\$2
Time to Verification /Diagnose One Defect	[min]	5	10	60	120
Time to Repair One Defect	[min]	15	30	50	50
Cost to Debug/Diagnose One Defect	[\$]	\$0.17	\$0.33	\$2.00	\$4.00
Cost to Repair One Defect	[\$]	\$0.50	\$1.00	\$1.67	\$1.67
ReTest Cost	[\$]	\$0.50	\$1.00	\$2.00	\$2.00
Cost of Field Failures/Returns	\$200	[\$]			
Current field return rate		0.0200%			


inspection strategy because it provides the only method to identify electrical faults such as component operation and component value. Only by considering all potential cost factors can the economics of ICT be optimized to deliver the lowest possible overall costs. The following example is based on the conditions faced by the typical low volume Asia assembler. This company produces a board with 800 components, 4,000 solder joints and a value of \$40 at a volume of 150,000 per year. The board has a repair yield of 85% and up to five repair cycles are permissible, yielding a calculated scrap rate of 0.0076%.

The electrical defect rate, expressed in defects per million opportunities (DPMO) is 250 parts per million components (ppmC) and the structural defect rate is 400 parts per million joints (ppmJ). The average number of structural defects per board is 1.6 and the average number of electrical defects per board is 0.2. **Table 1** shows the costs involved in each phase of the testing cycle. Note that the costs of verification/diagnosis, repair and retest increase substantially at each successive stage in the testing cycle, from ICT to functional test (FT) to environmental stress screening (ESS) to system test. This explains why overall costs can be reduced by identifying more defects in the early stages of testing and inspection when they can be diagnosed and repaired at a lower cost.


Now look at the performance of the ICT system in the context of FT, ESS and system test. The test access is the level of physical access that a test stage has to the PCB. In this case, we assume that the ICT has 95% test access, FT has 50%, ESS has 70% and system test has 80%. Fault coverage, on the other hand, refers to the effectiveness of a test stage in detecting a specific defect type on a location that is fully accessible. The test coverage is the product of fault coverage and test access. **Table 2** shows the assumptions that have been made for structural and electrical fault coverage for each stage of testing. The test coverage is the average of the structural and electrical test coverage weighted by the number of opportunities for error in each area.

Table 3 shows how costs accumulate and are distributed throughout the test and inspection cycle using the aforementioned assumptions. The chart calculates the total costs of verification, repair, scrap, retest and field failures – all the costs influenced


by inspection of testing – for conventional ICT with a structural fault coverage of 80% and an electrical fault coverage of 90%. These values are typical of today's ICT systems. Several important values should be noted on this chart. The overall test effectiveness, measuring by the proportion of defects detected by the tester, is 77%, so the DPMO remaining on the board after test is 86 and the first pass yield is 25%. The total annual test-related costs are \$453,722.




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Table 2. Test Coverage Assumptions

	ICT 1	TestStation	FT	ESS	System
Test Access	95%	95%	50%	70%	80%
Fault Coverage Structural	80%	85%	60%	90%	60%
Fault Coverage Electrical	90%	95%	85%	95%	99%
Test Coverage	78%	82%	32%	64%	53%
False Fail Rate [ppm]	50	25	10	5	2

Table 3. Total Test-Related Cost, Conventional ICT

	ICT	FT	ESS	System	
Structural Defects Before Test [per board]	1.6	0.384	0.2688	0.099456	
Structural Defects After Test [per board]	0.384	0.2688	0.099456	0.05171712	
Electrical Defects Before Test [per board]	0.2	0.029	0.016675	0.005586125	
Electrical Defects After Test [per board]	0.029	0.016675	0.005586125	0.001161914	
Structural Defects Found [per board]	1.2160	0.1152	0.1693	0.0477	
Electrical Defects Found [per board]	0.1710	0.0123	0.0111	0.0044	
Total Defects Found [per board]	1.3870	0.1275	0.1804	0.0522	
First Pass Yield	25.0%	88.0%	83.5%	94.9%	
Overall Test Effectiveness	77%	31%	63%	50%	
DPMO Remaining on Board after Test	86.0	59.5	21.9	11.0	Total
Annual Cost of Verifying	\$34,675	\$6,376	\$54,130	\$31,298	\$126,479
Annual Cost of Repair	\$104,025	\$19,129	\$45,108	\$13,041	\$181,303
Annual Cost of Scrap	\$741	\$80	\$93	\$28	\$943
Annual Cost of Retest	\$56,263	\$17,959	\$49,527	\$15,248	\$138,998
Annual Cost of Field Failures and Returns					\$6,000
Total	\$139,441	\$25,585	\$99,331	\$44,367	\$453,722

Table 4. Overall Testing Costs, Novel ICT Technology

	ICT	FT	ESS	System		
Structural Defects Before Test [per board]	1.6	0.308	0.2156	0.079772		
Structural Defects After Test [per board]	0.308	0.2156	0.079772	0.04148144		
Electrical Defects Before Test [per board]	0.2	0.0195	0.0112125	0.003756188		
Electrical Defects After Test [per board]	0.0195	0.0112125	0.003756188	0.000781287		
Structural Defects Found [per board]	1.2920	0.0924	0.1358	0.0383		
Electrical Defects Found [per board]	0.1805	0.0083	0.0075	0.0030		
Total Defects Found [per board]	1.4725	0.1007	0.1433	0.0413		
First Pass Yield	22.9%	90.4%	86.7%	96.0%		
Overall Test Effectiveness	82%	31%	63%	49%		
DPMO Remaining on Board after Test	68.2	47.3	17.4	8.8	Total	Savings
Annual Cost of Verifying	\$36,813	\$5,034	\$42,985	\$24,759	\$109,591	(\$16,888)
Annual Cost of Repair	\$110,438	\$15,103	\$35,821	\$10,316	\$171,678	(\$9,625)
Annual Cost of Scrap	\$726	\$68	\$76	\$23	\$893	(\$50)
Annual Cost of Retest	\$57,799	\$14,368	\$40,048	\$12,128	\$124,342	(\$14,656)
Annual Cost of Field Failures and Returns					\$4,795	(\$1,205)
Total	\$147,976	\$20,205	\$78,883	\$35,099	\$411,299	(\$42,423)

ICT Improvements

New ICT technology can increase both structural and electrical test coverage by 5% or more by addressing technological changes such as lower voltage thresholds that have reduced test coverage. The reduction in logic voltage thresholds has made

low voltage components more difficult to test reliably and more susceptible to damage from over-voltage and over-current test conditions. These conditions can occur routinely on conventional in-circuit testers and can cause low voltage devices to be destroyed immediately or damaged in ways leading to the early-life product failures in the field.

The recent increase in test coverage is based on the availability of ICT technology with higher levels of accuracy to

address the reduction in power supply voltages and transistor geometry. Driver accuracy of 45 mV and output impedance of less than 1 Ω means the driver is capable of accurately testing 0.8 V technologies and below under both no-load and backdrive conditions and is well-equipped to handle future low voltage devices. Automatic driver verification capabilities ensure that each driver achieves its programmed voltage value and improve diagnostics by identifying board conditions that prevent a tester driver from reaching its programmed value. In-circuit drivers perform real-time measurements of the backdrive currents and duration. This allows the tester to identify test conditions that require unusually large backdrive currents and highlight areas of the test program that have missing or inadequate device isolation steps. Per-pin programmable driver/sensor (D/S) pins allow the programmer and test generation software to assign logic levels appropriate for each pin on the device and avoid the compromises involved in sharing logic level assignments.

The resulting increase in test coverage and reduction in false rate can have a major impact on the overall costs. Using the same set of assumptions, **Table 4** shows the effect of substituting an ICT using the latest technology that provides a 5% improvement in structural and electrical fault coverage to provide

improved test coverage and reduced false failure rate. The number of defects found per board has increased from 1.3870 in the first example to 1.4725. This results in a first pass yield of 22.9% compared to 25% with the conventional tester. Overall test effectiveness has increased to 82% and the DPMO remaining on the board after test has fallen to 68.2.

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The annual cost of verification/diagnosis with the ICT has risen by over \$2,000 because the tester has identified more faults that must be diagnosed. On the other hand, total annual cost of verification/diagnosis is lower because costs have been reduced at the subsequent test stages. This is because more defects are identified and repaired at the relatively inexpensive ICT stage, leaving far fewer to be verified and diagnosed at higher cost in the downstream stages. Costs of repair at the ICT stage is also higher because the tester identifies more defects but the total costs of repair are lower because defects can be repaired at the lowest cost at the ICT stage. Retest costs are higher at the ICT stage and lower overall for the same reason.

The improvement in the cost of field returns shown in **Table 4** bears special mention. This improvement results from the reduction in DPMO remaining on the board after test from 11 with conventional ICT system to 8.8 with the new generation ICT. The reduction in DPMO is generated by the improvement in test access provided by the newer generation ICT. The field returns calculated based on this defect rate are much higher than those seen in the real world because many defects, such as redundant power connections, decoupling capacitors and unused parts, do not cause faults. The reduction in field returns was calculated in this example by comparing the DPMO in the two examples and applying the improvement in DPMO to the real field return rate seen with the conventional tester. The bottom line is savings of \$42,423 per year in overall costs affected by testing, a savings of nearly 10%.

Case study no. 2: High volume assembler. Now look at a different example to examine how the impact of the improved ICT technology varies from application to application. The new example is a high volume product produced in Asia with a solder joint count of 4,000, volume of 500,000 units per year, board DPMO of

375, \$2 labor costs, 15 min. repair time and a \$200 cost of field return. Using the same methods as the previous example, the ICT costs increased from \$464,804 to \$493,252 but the total test-related costs fell from \$1,512,407 to \$1,370,998; annual savings total \$141,409. In this example the calculated cost of field returns would have been \$5,287,903 with the conventional ICT versus \$4,226,273 with the newer generation ICT, although these numbers are much higher than what is seen in the real world for the reasons mentioned.

Case study no. 3: High complexity, low volume assembler. The final example involves a U.S. manufacturer of high value, low volume boards. The company produces 5,000 boards per year with a solder joint count of 12,000 and a board DPMO of 363. Labor costs are \$15 per hour, repair time is 15 min. and the cost of a field return is \$5,000. In this case, the ICT costs were \$114,588 with the older ICT and \$121,429 with the newer technology. The DPMO remaining was 10.1 with the older technology yielding field returns of \$25,000 per year while the DPMO was 8 with the newer ICT yielding field returns of \$19,935 per year. The total cost was reduced from \$359,896 with the older ICT to \$315,568 with the newer ICT, a savings of \$44,327.

These examples show how the 5% improvement in fault coverage achieved with the new generation of ICT systems can have a major impact on production costs. The two Asia examples both showed a savings of \$0.28 per board while the newer technology yielded a savings of \$8.80 for each high value board produced in the U.S. Careful attention needs to be paid to the effect of ICT performance on overall assembly costs to reduce assembly costs to the lowest possible level. ■

Michael J. Smith is chief technologist at Teradyne Corp.'s Assembly Test division (teradyne.com); michael.j.smith@teradyne.com.

**A 5% improvement
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