

Faster Shorts Testing

by Anthony Suto, Teradyne

As PCBs grow increasingly complex and lead-free solder technology dominates, test engineers will shift more attention to shorts and solder-joint integrity. Finding board shorts has become much more complicated due to reduced access, lower voltage rails, and other consequences of high-functionality designs.

A Look at the Problem

Testing for shorts presents two separate but related challenges. Lower-voltage technologies make detecting shorts more difficult while the sheer numbers of nodes on most of today's boards make the traditional one-to-many shorts testing technique unacceptably time-consuming—not to mention the possible damage to the board.

At its most basic level, shorts testing is an unpowered in-circuit analog impedance technique that can rapidly locate potential failures. Its ultimate goal is to prevent damage to the board that might occur if it were powered up for subsequent digital logic, boundary scan, and analog component testing with a short present.

Figure 1 shows the traditional in-circuit shorts test. A voltage source V_s supplies a stimulus to resistor R_x on the board under test. The current flows into a transimpedance amplifier or a current-to-voltage converter.

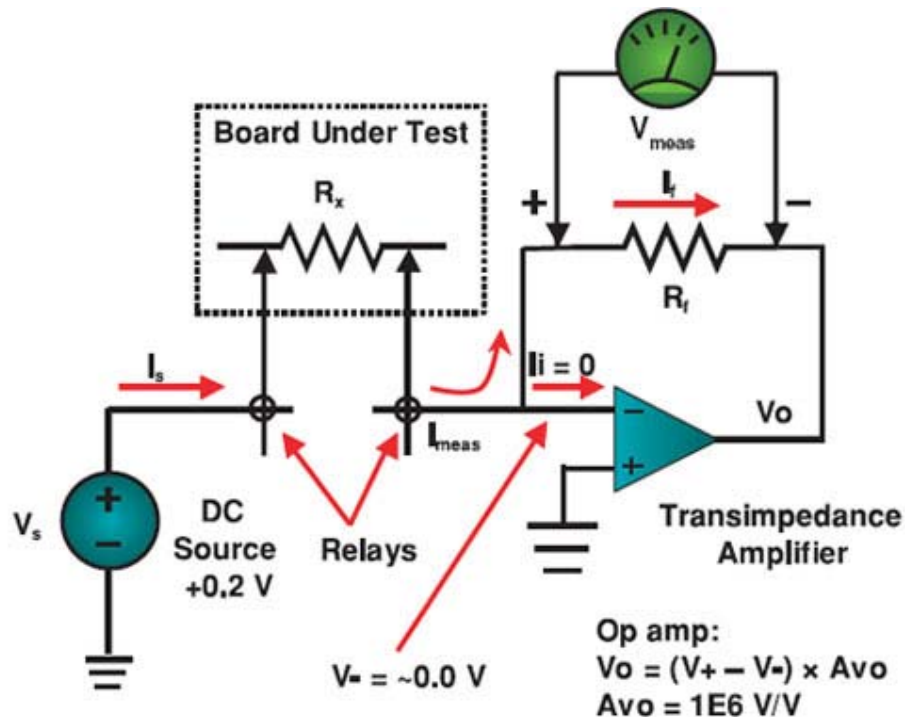


Figure 1. In-Circuit Two-Wire Resistance Test With Inverting Op-Amp Topology

Because of the test configuration, the bias current into the inverting terminal is negligible. On modern op-amps, it totals tens or perhaps hundreds of picoamps. So I_s essentially becomes I_f and propagates through R_f . The negative input to the op-amp behaves like a virtual ground:

$$I_s = V_s/R_x$$

$$V_{meas} = I_f R_f = I_s R_f$$

$$V_{meas} = (V_s/R_x)R_f$$

$$R_x = R_f V_s/V_{meas}$$

The unknown resistance equals the feedback resistance multiplied by the source voltage divided by the measured voltage. Most shorts testing is an adaptation of this simple two-wire resistance measurement technique.

Grouping the Nodes

Two procedures allow an in-circuit tester to locate all of a board's shorts. **Figure 2** shows the more common linear approach. In this case, the source voltage flows through a set of relays to an unknown resistance, then to the measurement node as before. All nodes are connected together through relays except for a single node under test.

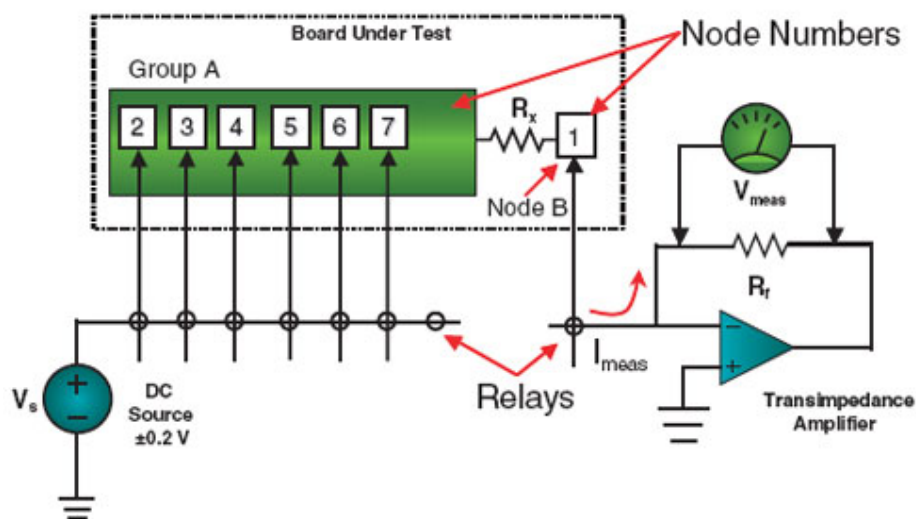


Figure 2. Basic Linear Shorts Test Method

Measuring for resistance determines if a short exists between the separated node, node 1 in this case, and the aggregate of the others. The test ensures that any measured resistance below a predetermined threshold value constitutes a short.

If a short is detected, node 1 is added to the shorted-node list. If not, the tester reconnects node 1 with the others and isolates the next node, such as node 2, to the measurement circuit to determine whether a short exists between that node and the new group. The cycle continues sequentially until all possible combinations have been measured.

Figure 3a shows the binary approach, which begins by dividing the board's nodes into two groups. This test connects Group A to the source voltage and Group B to the measurement channel of the transimpedance amplifier. Then it looks for a short between them.

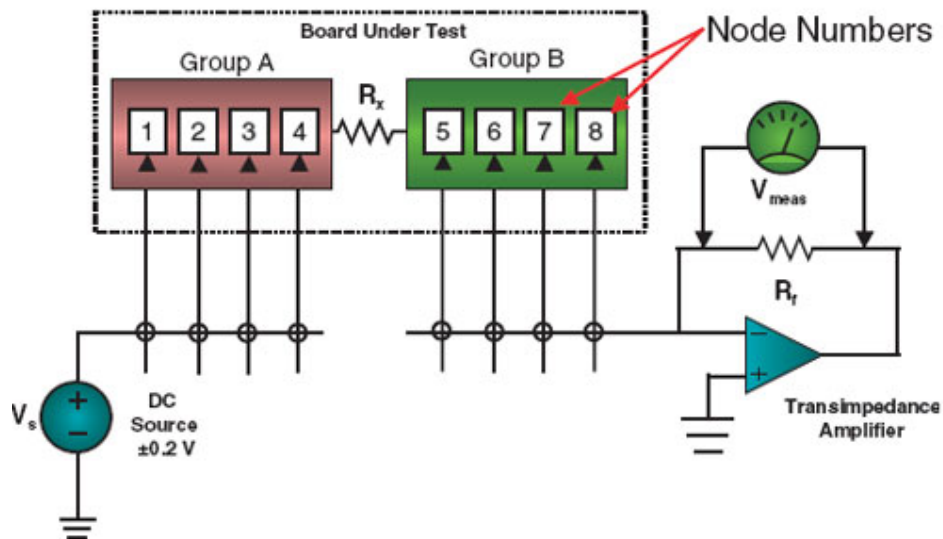


Figure 3a.

Assuming there are no shorts measured between these two groups, the tester reassigns nodes 1, 3, 5, and 7 to Group A and nodes 2, 4, 6, and 8 to Group B. As before, the idea is to determine if a short exists between any node in Group A and any node in Group B. Assuming no shorts are detected, the tester regroups the nodes into the arrangement shown in **Figure 3b**.

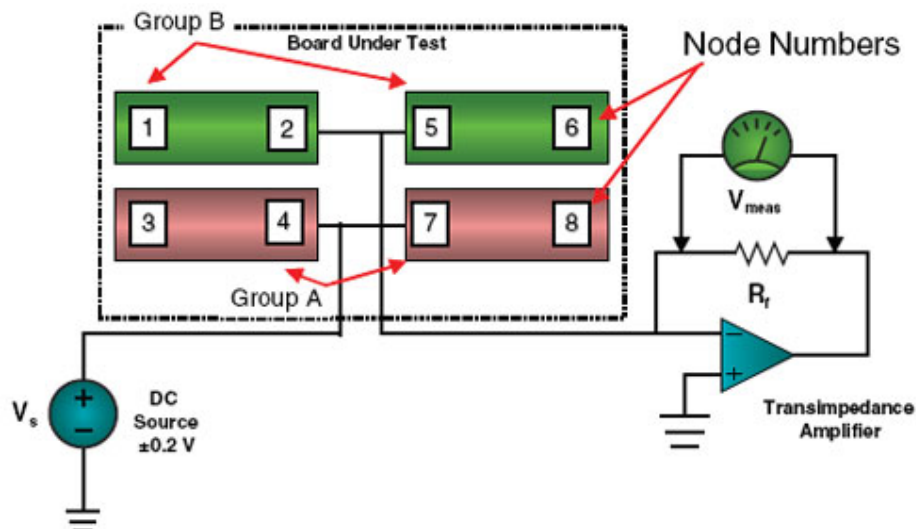


Figure 3b.

The binary test method required only three tests to determine whether there are shorts on the eight nodes. If no shorts are found, the routine ends. If the tester finds a short, it branches to another procedure that attempts to pinpoint which nodes are actually shorted.

Figure 4 shows the number of resistance tests required by each method to ensure there are no shorts on the board. The top curve represents the linear approach, which requires a number of tests equal to the number of nodes on the board (N). The binary method is more efficient, requiring only $\log_2(N)$ tests to determine if any shorts exist.

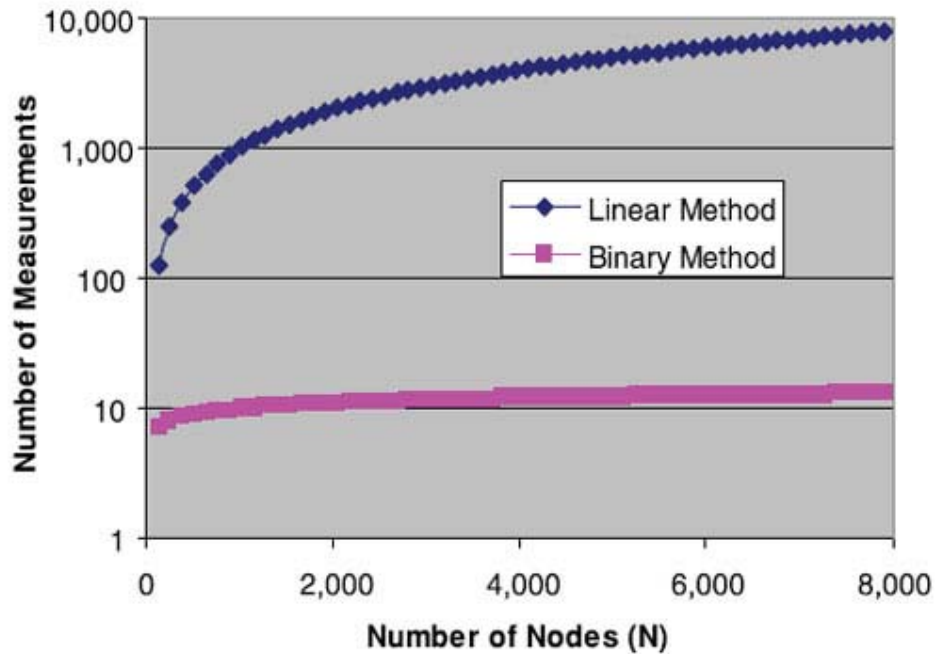


Figure 4. Linear vs. Binary Shorts Methods

Why Two Algorithms?

Unquestionably, the binary method is the faster method. Nevertheless, the linear approach can serve as a selectable prefilter to a second round using the binary method by determining which nodes are potentially shorted together. In that case, any nodes in the shorted-node list will be fed into the binary method test.

Using the linear method in this way can reduce the overall test time considerably. In particular, phantom shorts generated by components in parallel, such as 100 1-k Ω pull-ups or 10 100- Ω resistors that happen to be in the same group across those measurement pins, can present the tester an impedance low enough to look like a short even when there isn't one.

The binary algorithm believes that there is a short and starts going through its search routine, dramatically slowing it down. Eventually, as it divides the groups, the number of parallel components in each group declines to the point where the measured resistance increases and apparent shorts vanish.

The linear method allows the tester to eliminate nodes from consideration by creating the shorted-node list as input to the binary method. This scenario reduces the likelihood of phantom shorts and improves overall performance.

Demonstrating the power of the binary method is relatively easy if there are no shorts on the board. But consider the case of a faulty board, such as one with a short between nodes 1 and 9. The first binary test shows that the board has a short. The second test divides these groups into two separate blocks, one of which will exhibit the short. The algorithm then concentrates only on the shorted groups, dividing them again.

The resulting configuration permits four possible node choices that could produce the short. The algorithm then breaks out that combination further, conducting additional tests to demonstrate that the short indeed connects node 1 to node 9.

Resistance Thresholds

To identify a short, we generally set a default threshold value of 10 Ω . That is, the test calls any

resistance lower than 10 Ω a short. That threshold can be user configured from 5 Ω to 1kΩ although we recommend a maximum of 100 Ω to accommodate specific board architectures.

Our stimulus test voltage defaults to ±200 mV. We include both positive and negative voltages to address different semiconductor logic families. We recommend a voltage range between 50 mV and 200 mV although you can program it up to 16 V.

Obviously, we discourage such high levels for populated boards. Most Schottky diodes begin forward conduction between 150 mV to 450 mV at 1 mA while silicon P-N structures typically start to conduct between 600 mV and 700 mV at 1 mA. Nevertheless, higher voltages allow you to perform isolation testing on bare PCBs if you wish.

Programmability of the voltage source also allows this technology to safely and reliably test low-voltage components. Today’s devices run at much less than the 5 V or 3 V of years past. Digital devices may be based on 1.8-V or even 1.6-V logic. Providing test-system flexibility permits excellent fault coverage even when boards are based on such low voltages.

Capacitance

Large-value capacitors in parallel with the nodes under test, as in **Figure 5**, can cause problems. Waiting for them to charge and discharge to assure accurate measurements can take an inordinate amount of test time.

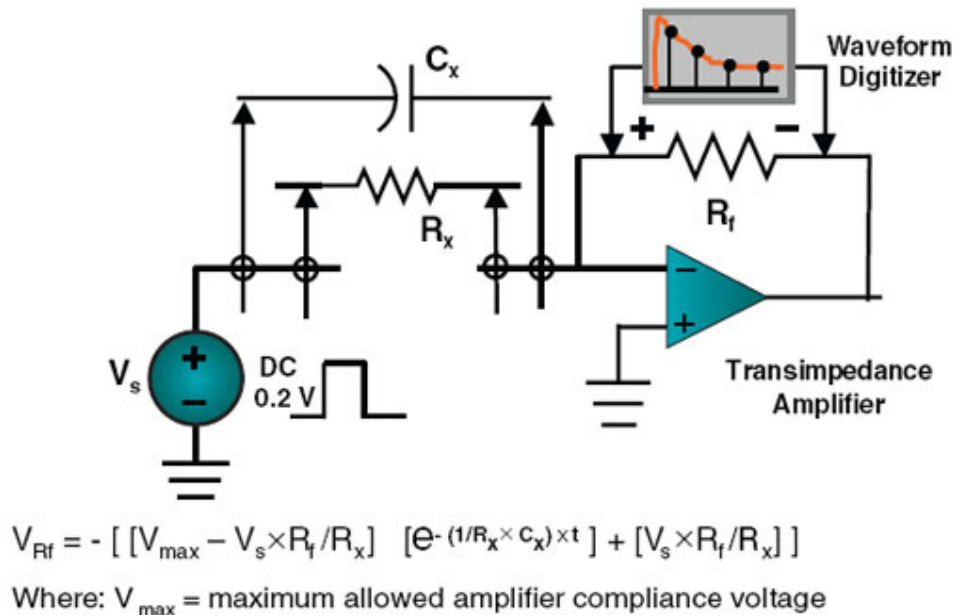


Figure 5. Transient Test for Large Capacitors

To shorten that time, we anticipate the circuit’s behavior. The tester digitizes the transient waveform that occurs when we first close the DC source, analyzing the initial voltage spike and subsequent exponential decay. The decay rate depends on the RC time constant, as the waveform equation in Figure 5 shows.

The maximum value of the amplifier output relies upon the device power supply and the input compliance settings. Our software attempts to predict the final resistance value and whether it will be above or below the shorts threshold, reducing the test time to make the short/no-short decision.

We could simply remove these tests because they are too slow; however, we do not because that would sacrifice fault coverage. You typically find large-value capacitors across power supplies where the possibility of shorts represents a particular concern.

Inductors

Inductors present another type of challenge. These components typically have very low DC series resistance; as low as 0.1 Ω , 1 Ω , or 5 Ω is not uncommon. If we examine them using the traditional shorts test, they surely would fail. At higher AC frequencies, however, the imaginary term of the complex impedance dominates, and the overall magnitude of the inductor's impedance rises.

In our case, our automatic program generator pulls inductors, low-value resistors, fuses, jumpers, and other low-impedance components from the initial list by opening one of the relays that connects either of their terminals to the measurement nodes. Surprisingly, that approach increases fault coverage because, with those components connected, the remaining nodes in parallel would become untestable.

False Failures

Depending on the shorts threshold or the source voltage, semiconductor devices across certain nodes may appear shorted, causing false failures especially if the source voltage is high enough to turn on hot-carrier diodes or some Schottky barrier diodes. At that point, we still don't know if it is a hard short.

To clarify the situation, the shorts algorithm reverses the polarity on the measurement to see if the short persists. If so, it is a true short, helping to eliminate false calls that you would otherwise experience.

Low-impedance resistors across certain nodes also can look like shorts. As the binary algorithm divides them into smaller and smaller groups, it assigns fewer and fewer of those resistors to each group.

At some point, the resistance value will rise above the shorts threshold, and the tester will no longer see it as a short. When that happens, the algorithm runs the test a predetermined number of times to ensure that the short really is just a phantom short and the final passing condition is not caused by extraneous noise.

Hipot Testing

Some customers like to test bare boards on in-circuit testers. More recently, some people have begun testing ceramic or multichip carriers or just plastic over-molded BGA packages that have C4 flip-chips on them. Manufacturers don't want to attach expensive die material to substrates when they don't know if the substrates themselves are good.

Companies have approached us to provide a hipot test for these types of devices at in-circuit test. We offer a source voltage up to 120 V for testing unpopulated boards, generating measurable current through this very high leakage impedance.

Conclusion

The inconvenience of finding shorts on today's crowded, limited-access, low-voltage boards doesn't negate the necessity of doing so. Combining linear and binary techniques during in-circuit test can dramatically reduce test times and increase throughput as can predicting the voltage patterns for high-value capacitors. Effectively identifying shorts at in-circuit test can lower overall test costs because it reduces the likelihood of causing collateral damage when powering up boards or having the faults surface during later test steps when repairing them is more expensive.

About the Author

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