

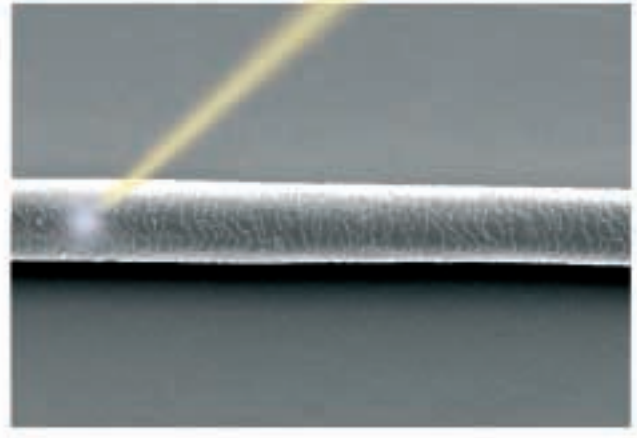
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**JUNE 2002**

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# Combining ICT And Boundary Scan Testing

by Alan Albee,  
Teradyne ATD

A joint ICT/BSCAN test strategy proves to have several advantages over a boundary scan only test strategy. A look at these benefits and the board testability and design issues that must be considered to provide a comprehensive ICT/BSCAN solution.

In-Circuit Testing (ICT) has long been the number one testing method for most high volume manufacturers of electronic systems. The main reason for this preference is that, among other benefits, it offers the tester access to practically every component pin on the unit under test (UUT). However, it is becoming increasingly more difficult and expensive to design In-Circuit fixtures to access component pins on advanced products featuring ever smaller board geometries. Consequently, many manufacturers have turned to a boundary scan test strategy to solve the problems caused by the loss of test access. Some have turned to benchtop boundary scan test solutions, but find that these cannot provide the same level of fault coverage, throughput, and diagnostic accuracy as traditional ICT.

An ideal compromise is to combine boundary scan test techniques along with traditional ICT methodologies, which allows the testing of inaccessible nets and the purchase of less expensive reduced probe count test fixtures.

## Benchtop BSCAN testers

Benchtop boundary scan testers typically perform only boundary scan tests and can miss a significant percentage of the manufac-

turing defects that occur on a board and which are detected by in-circuit testers.

The following cases represent some typical examples:

- *Shorted Nets* - Benchtop boundary scan testers can reliably detect shorts only on pure boundary scan nets. Shorts between boundary scan and non-boundary scan nets will only be detected when the non-boundary scan net is not in a high impedance state. Even if the short is detected, benchtop boundary scan testers cannot provide accurate diagnostic information to aid the repair. Detecting all possible UUT shorts is an important benefit of the combined ICT/BSCAN test strategy.

- *Mixed Component Nets* - Benchtop boundary scan testers cannot detect faults on boundary scan nets that also have a connection to conventional digital tristate or bidirectional pins. These mixed component nets must be removed from the boundary scan tests resulting in reduced fault coverage. A combined ICT/BSCAN test strategy allows these mixed nets to be included in the test. This is because the conventional tristate and bidirectional pins are preconditioned using the ICT Driver/Sensor technology prior to the Interconnect test.

- *Missing or Faulty Parts* - Benchtop boundary scan testers cannot detect missing analog parts or conven-

tional digital parts that do not have access to virtual boundary scan drivers and sensors. With most board designs, this can result in a significant loss of test fault coverage. By providing 'bed-of-nail' access to the nets that contain these parts, and using standard In-Circuit test techniques, missing or faulty non-boundary scan parts can be detected.

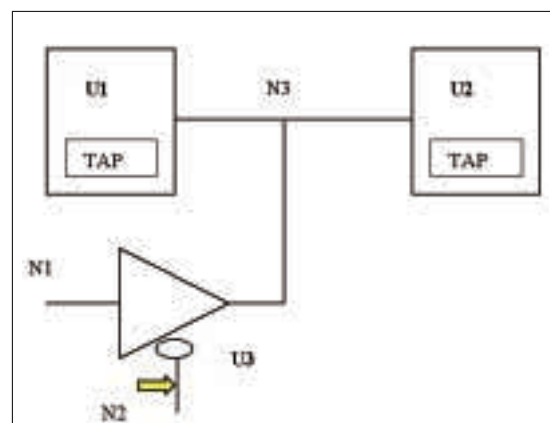
## Other Benefits of ICT

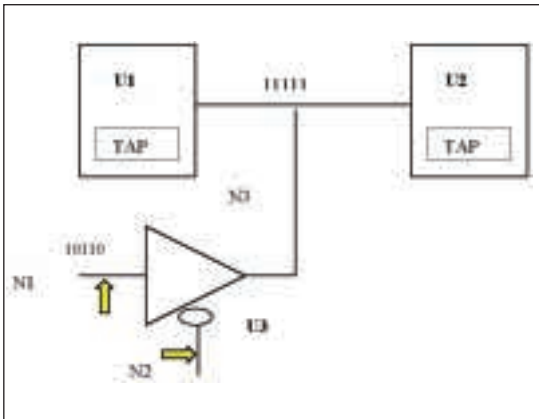
In-Circuit testers come equipped with a number of standard hardware features that are not available in benchtop boundary-scan testers. These hardware features can be used to simplify program development and extend the fault coverage of boundary scan tests.

## Driver/Sensor Technology

Most In-Circuit testers have sophisticated Driver/Sensor technology that can be used in combination with the boundary scan

*Figure 1 - Net N3 cannot be tested during the boundary scan interconnect tests unless the output from conventional component U3 can be shut off. Using a combined ICT/BSCAN tester, the U3 output is disabled by driving N2 high with an ICT Driver/Sensor nail*





*Figure 2 - A short between nailed conventional net N1 and un-nailed boundary scan net N3 can be detected by programming the U1 boundary scan output to drive all ones, and by driving a unique identifier on N1 using the tester Driver/Sensor nail. If the U2 boundary scan input captures the N1 identifier, instead of all ones, then a short exists between the two nets. This test technique relies on the fact that the driver technology has enough current capacity to backdrive the boundary scan outputs. During the test, U3 is effectively disabled by driving net N2 high with a tester Driver/Sensor nail*

tests to provide the following benefits:

- In-Circuit Drivers can supply very high drive currents, usually greater than 500mA, that can be used to backdrive, or force, device nodes to the voltage required by the boundary scan tests. This is fundamental to boundary scan interaction tests, which are used to detect shorts between nailed conventional nets and un-nailed boundary scan nets (see figure 2).
- The high current capability of the In-Circuit Drivers can be used to avoid programming scan path selector and bridge devices: the Drivers can directly backdrive the outputs of these devices.
- In-Circuit Drivers can be used to drive multiple UUT scan paths simultaneously.
- Most In-Circuit testers have hundreds, if not thousands, of Driver/Sensor pins. These drivers can precondition critical UUT signals prior to the start of the boundary scan tests. The drivers can also be used to ensure that non-boundary scan components are shut off so

that they do not interfere with the boundary scan tests. Special tooling boards must be designed on benchtop boundary scan testers to accomplish the same objectives.

- In-circuit drivers and sensors can supplement targeted virtual pin testing of conventional digital components. Benchtop boundary scan testers are only able to test conventional digital components when all the pins of the conventional component are con-

connected to a boundary scan pin that can act as a virtual driver or sensor. Combined ICT/BSCAN testers can test otherwise untestable components by driving and sensing the pins that do not have boundary scan access with tester Driver/Sensor nails.

- Most In-Circuit Drivers have programmable voltage values. Programmable drive levels and slew rate controls also help when trying to debug electrical problems related to ground bounce or ringing TAP signals.

#### Automatic Isolation

Most In-Circuit testers have Automatic Test Generation (ATG) software that is used to generate tests for components on the board and relies on device libraries describing how to test and isolate individual components.

Combined ICT/BSCAN testers can take advantage of the built-in ATG software to isolate all conventional UUT components during the boundary scan tests, minimizing false failures during the boundary

scan tests due to non-boundary scan device interference.

#### Analog Stimulus and Measurement Instruments

In-Circuit testers come equipped with analog stimulus and measurement instruments that are not available on benchtop boundary scan testers. These instruments can be scanned to any D/S resource in the tester so that instrument connections do not have to be hardwired in the test fixture.

Combined ICT/BSCAN testers can make use of these instruments to improve fault coverage and the diagnostics of the test program.

#### Programmable UUT Power Supplies

In-Circuit testers come equipped with power supplies that can program voltage and current parameters for the board under test. This capability allows automatic generation of safe UUT power-up, power-down, and discharge routines. Most benchtop boundary scan testers do not provide programmable power supplies, and the UUT must be powered up using separate, stand-alone power supplies.

#### Automation Ready

Features of the ICT, like vacuum or compression actuated fixtures, paperless repair software, data logging software, panel test software, and compliance to SMEMA specifications enable testers to adapt to the highest throughput automated manufacturing facilities.

#### Debug Issues

One of the advantages of boundary scan testing compared to traditional in-circuit vector testing is that, provided the information about the testability circuitry is correct (BSDL), and the boundary

scan components comply with the IEEE 1149.1 standard, then the program developed will work without debug. This is due to the fact that the boundary scan test software knows how all boundary scan components will behave when they are in test mode.

Boundary scan tests rely on all devices in the chain being compliant and described correctly. A single non-compliant device or inaccurate BSDL description can cause all boundary scan tests to fail.

The boundary scan debug process is much different than traditional in-circuit debug. Having test point access to all nets, as in in-circuit test, makes debug a simpler process than when only partial net access is available. The person doing boundary scan debug must not only have a good understanding of in-circuit debug techniques but also a knowledge of the boundary scan IEEE 1149.1 specification and of the hierarchy of boundary scan tests generated by the boundary scan software.

The person assigned to debug combined ICT/BSCAN tests must use a block diagram approach to 'bringing up' the board and must rely on test sequence knowledge to logically determine possible causes of boundary scan test failures. The most common reasons for boundary scan test failures are listed below, along with the debug actions that can be used on combined ICT/BSCAN testers to resolve them.

### **BSDL Inaccuracies**

A BSDL model contains many facts about what the test circuitry in the boundary scan part does. A typical 250-pin boundary-scan part will have about 400 facts in the BSDL model. Any fact being wrong can cause one test (or many tests) to fail.

Finding mistakes in BSDL models with loaded board tests is difficult, particularly if the board has many

boundary scan devices. Unless there is very good reason to be certain that the BSDL is correct (e.g. it has been produced automatically by a synthesis tool and never altered, or it has been used with success on other boundary scan tests) it should be regarded as untrustworthy.

To avoid complex debug activities caused by inaccurate BSDL models, each BSDL model should be verified by generating boundary scan tests to test a single device. In-Circuit testers usually offer BSDL verification software. The BSDL verification software is capable of detecting a mismatch between device behavior and data facts in the BSDL model.

### **Isolating Conventional Components**

As shown in Figure 1, boundary scan nets that are connected to conventional digital output or bidirectional pins can fail boundary scan Interconnect tests. This occurs when the conventional digital output driver is not shut off and conflicts with the value that the boundary scan output is attempting to drive the net.

In order to reliably test these nets, the conventional digital output or bidirectional pins must be effectively disabled by placing them in a high impedance condition. In-Circuit testers also have software libraries for common commercial components that describe how to isolate or disable device pins. So, if the tester has access to the control pins of a conventional component, and a model for the component is present in the device libraries, then the automatic test generation software can automatically include the appropriate isolation sections.

When the tester does not have access to the control pins of the conventional component, then these nets can not be reliably tested and the test programmer must remove them from the boundary scan tests. If the tester has access to the control pins, but is missing isolation

sections because a device model for the conventional component does not exist, then the boundary scan test is likely to fail or be intermittent. In this situation, the test programmer can create a device model for the conventional component that includes isolation information, or add the isolation code directly to the test program during debug to resolve the problem.

### **Electrical Problems**

The boundary scan TCK signal is an essential part of the test equipment that is testing the PCB. If TCK is noisy, ringing, or otherwise unreliable, many tests will fail badly. Electrical problems that affect boundary scan tests usually fall into one of two categories:

- **Ground Bounce** - This electrical problem is caused by bad component design, or by a poor power and ground distribution in the board or fixture. Boundary scan tests are the ones most likely to bring ground bounce susceptibility into the open, because boundary scan tests, by their very nature, will change many device outputs at the same time. In addition, shorts to un-nailed nets may be discovered when changing device outputs, which can cause large current changes that were not anticipated by the designer.

There is in fact no way for any test generator to avoid unlimited numbers of simultaneous changes because the change into EXTEST operation is a change from normal operation (when the boundary scan hardware is transparent) to EXTEST (where the device outputs are controlled by the boundary scan hardware).

- **Signal Reflections** - Digital transmission line theory teaches that as the frequency and slew rate of a digital signal increase, the more likely it is for ringing to occur, and the more important it is to have matched network impedances to prevent signal reflection.

Defect	BSCAN Only	ICT Only	Combined ICT/BSCAN
Shorts between unnailed Pure Bscan Nodes	✓		✓
Shorts on unnailed mixed component nets			✓
Shorts between unnailed Bscan nets and nailed non-Bscan nets			✓
Shorts between nailed non-Bscan nets		✓	✓
Opens on unnailed Pure Bscan nets	✓		✓
Opens on nailed single pin Bscan nets		✓	✓
Missing or faulty non-Bscan parts	Only if non-bscan part can be tested using bscan pins as virtual drivers and sensors	✓	✓
Missing or faulty Bscan parts	✓	Only if bscan parts are nailed	✓
Fixture Cost / Diagnostic Accuracy			
Fixture Cost	Low	High	Medium
Diagnostic Accuracy	Poor. Cannot diagnose faults on non bscan nets	Excellent, but all nodes must be nailed	Good. Can diagnose faults on nailed and unnailed nodes

Table 1 - Test fault coverage, fixture costs and diagnostic information comparison

If the TCK signal is being driven by the output of an on-board device, then it may have a very fast slew rate that can cause ringing. If the TCK net is attached to a tester D/S resource, then the ringing effect can be magnified by the effects of the fixture wire attached to the net. This problem can be resolved in several ways on combined ICT/BSCAN testers. If you have access to the TCK signals, you can disable the output pin that is driving the TCK signal and drive the TCK nets directly with the tester D/S resources. This approach allows the test programmer to control the slew rate, voltage, and frequency of the TCK signals for best results. If the above approach cannot be used, then the test programmer can remove the fixture wire(s) attached to the TCK signal(s) to reduce signal reflections caused by the wires that are attached to the net.

### Non-Compliance

Boundary scan tests and the pertinent methods are based on an important assumption: that there is correctly functioning boundary-scan circuitry in the components (devices have to obey the IEEE 1149.1 Standard). Unfortunately

there are a significant number of devices that fail to adhere to the Standard, and often the problems this causes are regarded as problems with the test tools, rather than with the components.

Non-Compliant parts can easily mean that there is no chance of using a boundary-scan based test strategy, or that excessive work will be needed to implement such a strategy. It is often hard to discover non-compliance from vendor documentation. One place that non-compliance is sometimes documented is in comments in BSDL descriptions.

There are three general strategies for handling non-compliance: modifying the BSDL file to describe a compliant subset of device behavior, altering the tests that are produced by the test generators, or modifying the board circuit description.

### Access Decisions

To obtain the benefits of a combined ICT/BSCAN test strategy, you must determine where access is critical and build a test fixture to provide access to the critical component

pins on the UUT. The amount of access required, and the complexity of the fixture will depend on the amount of pure boundary scan nets on the board and what your test strategy is for testing non-boundary scan components.

Some ICT vendors provide software that analyses board designs and produces reports that help to make access decision tradeoffs. In general, access should be provided to Test Access Port nets, Compliance Pins, non boundary scan nets, critical UUT control signals and intermediate TDI/TDO nets on the PCB.

### Summary

Manufacturing densely packed Printed Circuit Boards with boundary scan components allows test engineers to maintain high fault coverage with limited test access. However, test solutions that only employ boundary scan test techniques can cause many manufacturing defects to escape detection. Table 1 shows that a test approach that combines boundary scan test techniques with traditional In-Circuit test techniques provides the best test fault coverage and most accurate diagnostic information.

**For more information please contact:**

**Teradyne GmbH  
Renate Fritz  
ATD Marketing Communications – Europe & Asia  
Ismaning, Germany  
Phone: +49 89 962 85 303  
e-mail: [renate.fritz@teradyne.com](mailto:renate.fritz@teradyne.com)**

**Teradyne Inc.  
Mark Stygles  
ATD Marketing Communications – North America  
Westford, MA 01886-0033, USA  
Phone: +1 978 589 7425  
e-mail: [mark.stygles@teradyne.com](mailto:mark.stygles@teradyne.com)**

**[www.teradyne.com](http://www.teradyne.com)**

