

Cray Research beats the market with boundary scan

“Prototype boards are now cleared of physical faults in hours rather than days.”

How much time can boundary scan save in getting new products to market?

Jeff West, a senior test design engineer at Cray Research, says, “By adding IEEE 1149.1 circuitry and using commercial-off-the-shelf tools, prototype boards are now cleared of physical faults in hours rather than days. This saves weeks in the checkout of prototype systems. Manufacturing can now deliver many more boards per day to system checkout with confidence that boards are defect-free.”

Cray Research, headquartered in Eagan, Minnesota, with a primary design and manufacturing center in Chippewa Falls, Wisconsin, builds supercomputers for technical and business applications. The CRAY J90 series is the third generation of Cray Research’s low-cost supercomputer. The CRAY J90 systems are high-speed, high-density computer systems based on CMOS technology.

The CRAY J90 was designed and tested with IEEE Std 1149.1 circuitry. Its predecessor the CRAY EL90, circa 1992, was not. Prototype board debug on the CRAY

EL90 took three to five days and manufacturing test could take as long as two days.

The CRAY EL90 was tested on a homegrown tester designed to find physical board faults. For prototype test, diagnostics were run on sections of the board. To further diagnose errors, technicians probed the board to narrow down the location of errors while looping on a piece of code that was known to cause a certain failure.

“With this probing method, it could take anywhere from a couple of days to more than a week before a prototype board was completely defect-free,” says West.

In the generation between the CRAY EL90 and the CRAY J90 series, Cray engineers saw an increase of circuit density by a factor of two to three times (Figure 1). Without a quick, efficient, and cost-effective solution to test the CRAY J90 boards, Cray ran the risk of missing the market window for this new product. “Even if prototype boards could have been delivered on time,” continues West, “manufacturing costs would have

risen dramatically in our effort to find possible physical board faults.”

A new design-for-test approach

Ten new ASICs were designed for the CRAY J90 with 350,000 to 800,000 gates each. These are used on two board types, a central processor module and memory module.

Boundary-scan circuitry was designed into 100 percent of the I/O pins of each ASIC, which made it possible to check all the system nets on the CPU board and all the nets on the memory board, except for the nets to and from the DRAMs. Approximately two percent of the available gates per ASIC were used by boundary-scan circuitry.

In addition to designing in boundary-scan technology at the board level, the Cray Research team added a maintenance ASIC to each board for system-level boundary-scan test. Space for the logic was found on the clock distribution ASIC, which was designed as one chip with two jobs. Two copies of the chip were added to the system-clock board, one for system-clock fanout and the other for maintenance control of the system. The functions were separated on the clock distribution ASIC so that the maintenance logic would not induce noise into the clock logic.

For system-level test, the logic on the clock distribution maintenance ASIC, or the MC chip, was designed to work as either a master or slave. The master MC resides on the system clock board. This is an independent board connected to the

	CRAY EL90	CRAY J90
CPU board nets	2,731	4,801
Memory board nets	3,200	9,502
Backplane nets	2,227	5,432
ASIC gate counts	50,000	800,000
ASIC I/O pins (max.)	250	425
ASICs — CPU	23	20
ASICs — memory	9	44

Figure 1. CRAY EL90 vs. CRAY J90 density comparison

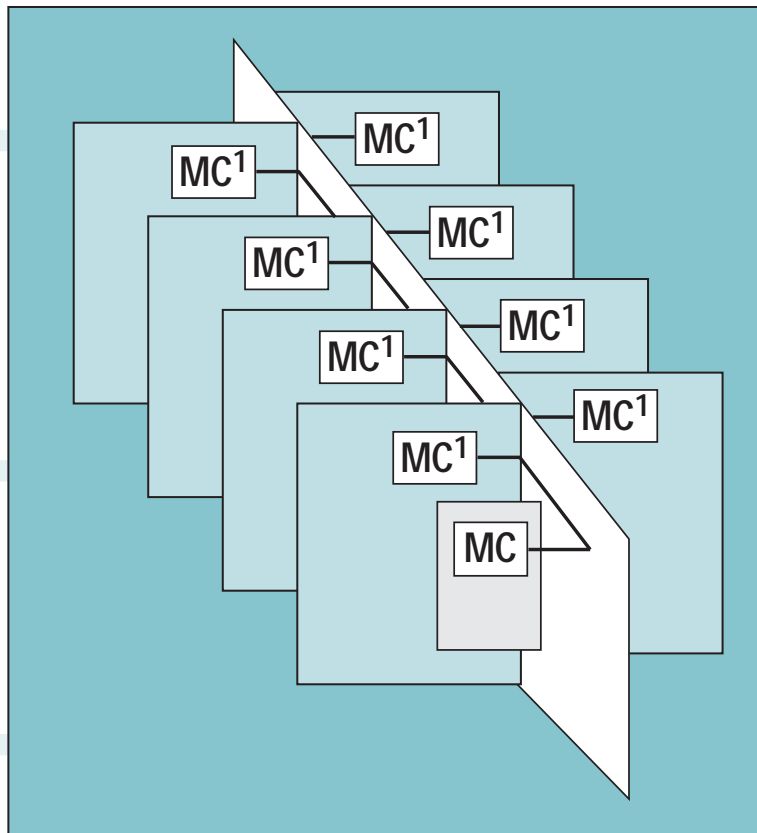


Figure 2. CRAY J90 system boundary-scan control routing

backplane, which receives signals from the maintenance channel connected to a workstation. A slave MC, or MC-1, was added to each CPU and memory board. MC-1 receives boundary-scan signals from MC and then fans them out. Cray Research's design did not require the system clock to run boundary-scan tests at either the board or system level (Figure 2).

"In order to design these 10 high gate-count ASICs and keep our aggressive schedule, design-to-test methods like boundary-scan needed to be implemented with the least impact to the designer," says West.

To reach this goal, hierarchical design methods were devised where the 1149.1 logic was fully contained within its own level of hierarchy. "All the logic designer needed to do was supply the I/O test port connections to the top level of the logic," says Dave Meinen, a

colleague of West. "Synthesis scripts were written that would add the boundary scan logic after the designer had completed the design. Logic and timing simulations verified the correct insertion of the test logic, insuring that no system timing constraints were violated."

Putting it to the test

To test these new boundary-scan designs, Cray Research developed a VXI-based test system using Texas Instruments' ASSET™ diagnostic system.* With boundary-scan logic built into the CRAY J90 ASICs, physical defects were found at one time on one tester, as opposed to the iterative approach used on its forerunner, the CRAY EL90. "We are now able to find all the physical defects on a board in less than 15 minutes," says West. Although Cray Research-specific variations of the IEEE standard had been considered, the advantages of using third-party hardware and software for testing

swung the vote in favor of using the IEEE 1149.1 protocol.

Bringing up a prototype — Cray supercomputer

The Cray J90 prototype boards were built in stages as the ASICs became available from Cray's outside vendor. Test vectors were generated with VICTORY's Virtual Interconnect Test software (VIT). "Vectors were created in a matter of minutes, depending on which ASICs were available," says West. To test partially populated boards, a jumper wire from the last ASIC's Test Data Out (TDO) pin to the TDO pad of the missing ASIC connects the scan chain and testing resumes.

To test backplane nets, output signals were looped back to the input signals. Any unmatched inputs or outputs were run to a VXI boundary-scan board, which connects to the serial boundary-scan chain. Using the VXI board meant that 100 percent of the backplane signals could be tested.

As more of the ASICs were added to the CPU and memory boards, a series of IEEE Std 1149.1 tests could be run on the in-house developed boundary-scan tester.

The TAP-controller test captures and scans the output of the 1149.1 instruction register. According to the IEEE standard, the first two bits captured from the instruction register should have a 1 in the bit 0 position and a 0 in the bit 1 position. By scanning this data, Cray Research engineers confirmed that the TAP controller was working correctly on all ASICs and the Test Data In (TDI) to TDO connections between each ASIC were properly connected. Returning TDO data is then checked for the right output.

*Now marketed by Asset Intertech, Inc.

“With this check, we are able to see any problems that may exist between the ASICs’ TDO-to-TDI connections,” says West.

A third test reads each ASIC’s 1149.1 ID register. Cray Research uses a 32-bit register to store identifying data such as the part number, revision level of the part, and the foundry code. This test allows the test engineer to verify that each ASIC type is in the right position on the board and that the correct revision is being used.

The ASIC I/O connections are tested with the IEEE 1149.1 EXTEST command. VICTORY-generated test vectors are run through the board-under-test and the results analyzed with ASSET software. If shorts and opens are detected, a list of failing I/O pins and ASICs is produced.

By using boundary-scan, Cray Research cut prototype testing by seven weeks. Since physical defects could be quickly diagnosed on system boards, functional debugging on prototype boards could start in as little as one day after a memory and CPU board were received from assembly.

Hierarchical design benefits

“Our plan to make boundary-scan hierarchical has paid large dividends,” says West.

Test engineers have the ability to stop a system and run boundary scan tests on either the complete system, an individual board, or the

backplane nets, whenever data indicates that failures are caused by physical defects. “The entire J90 system of eight boards with 16 CPUs can be run and failing nets analyzed in less than two minutes,” continues West. “You can imagine the benefits of this speed when Cray is shipping 40 to 50 of these systems a month.”

The hierarchical boundary-scan capability saves time in field repairs as well. “Historically, greater than 95 percent of system failures in the field are the result of physical board or connector problems. Our Cray Research engineers can now run boundary scan remotely from a customer site, so field support engineers know immediately which board, chip, or connector is defective. Spares or replacement boards can be swapped with defective boards in minutes,” says Karne Beighly of Cray’s Engineering Diagnostics group.

Since its initial shipment in March, 1995, more than 150 CRAY J90s have been shipped to customers. “This blows away all Cray Research records,” says West. The Cray J90 went from prototype to full production in just two and a half months.

So, yes, boundary scan can save time — even when manufacturing supercomputers. ■



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Printed in U.S.A.