# Hierarchical Test Generation: Taking Boundary Scan to the Next Level

**Peter Hansen**
VICTORY Software Development Manager
Teradyne, Inc.
Boston, MA 02118
Phone (617) 422-3496 Fax (617) 422-3100 E-Mail: peter.hansen@teradyne.com

***Abstract — Development of the original IEEE 1149.1 boundary-scan standard in 1990 was motivated primarily by concerns about the complexity of testing increasingly dense printed-circuit board assemblies in manufacturing. As a result, most test generation efforts have been targeted at unit test, which is most applicable to testing MCMs and boards. As boundary-scan technology has matured, there is a new focus on extending the technique to testing all levels of an assembly's hierarchy, at all phases in its life cycle.***

## I. INTRODUCTION.

For the past 20 years, bed-of-nails test using in-circuit test (ICT) techniques has dominated testing and diagnosis of structural faults on boards. Fine-pitched device packages such as Tape Automated Bonding (TAB) have threatened the usefulness of bed-of-nails fixtures, but the actual loss of physical access at the board level has taken longer than expected—in part because of the lack of practical high-density packages, in part because of the immense ingenuity of the fixture industry. However, the popularity of new high-density, area array packaging techiques such as the Ball Grid Array (BGA) will soon bring an end to the era of nearly universal access. As that occurs, boundary scan is taking the place of ICT in testing the digital portion of a board.

MCMs have never really enjoyed the efficiencies of ICT, relying instead on functional test techniques to find structural faults. As valuable as functional test is in detecting operational problems within an assembly, it is not an efficient way to find common structural fault types: stuck-ats, opens, and dead pin I/Os. As the functional complexity of MCMs continues to increase, boundary scan is the only solution for cost-effective structural test [1, 2].

Today, there are numerous examples of test developers working on extending the use boundary-scan techniques. One focus of interest is MCMs and military assemblies, where internal physical access has always been limited. Another is testing at the box and system level. Under the ARPA Application Specific Electronic Module (ASEM) program, test developers are also working on issues such as test portability and reuse that are essential to successfully addressing test at all assembly levels and at all phases of the product life cycle.

There are two boundary-scan test techniques that can detect and diagnose structural faults in digital circuits that have edge-connector-only access: Virtual Interconnect Test (VIT) and Virtual Component and Cluster

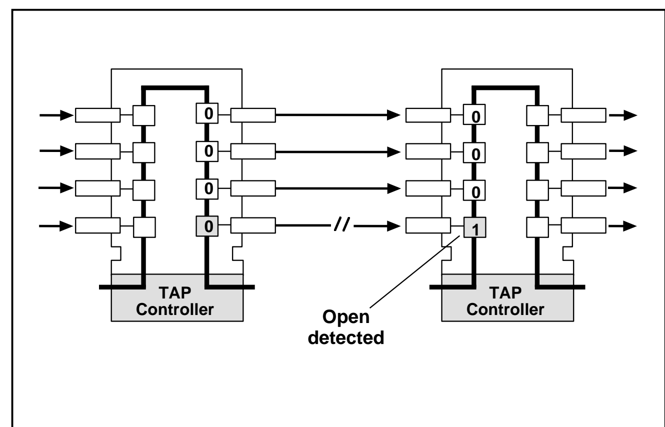


**Figure 1. Sample VIT test scenario**

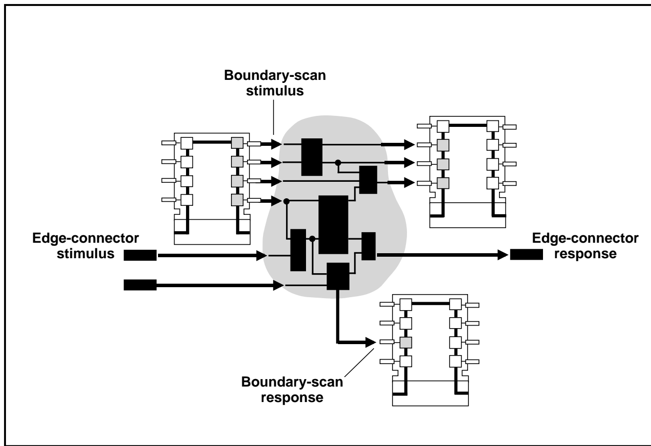


**Figure 2. Sample VCCT cluster test scenario**

Test (VCCT) [3]. As shown in Figure 1, VIT detects faults in the interconnections between boundary-scan device leads. VCCT detects structural faults in a single conventional device or in a cluster of conventional devices (as shown in Figure 2) that is surrounded by boundary-scan logic [4]. Since VIT tests scan-only interconnections, test generation can be fully automated and diagnosis is very precise. VCCT uses static functional test techniques that are less automated than VIT, but much simpler than conventional functional test of an entire assembly. Both of these techniques can be applied not only at unit test, but also at any higher level of assembly. In addition, VIT and VCCT techniques can be used throughout a product's life cycle, from prototype debug to depot test.

## II. UNIT TEST.

The most common view of boundary-scan technology is that testing is performed by simple five-wire ATE connected to the TAP of the unit-under-test. While test-generation software can be adapted to work within this limitation, five-wire ATE cannot test the nets associated with the unit's I/O. To achieve full fault coverage at unit test, you need to be able to stimulate and observe I/O pins—potentially hundreds of I/O pins—with ATE channels. When the unit is installed into the next level of the assembly's hierarchy, the assembly itself can provide control and observability on the unit's I/O for full fault coverage.

Apart from the issue of reduced fault coverage, five-wire, TAP-only test is often the most pragmatic starting point—offering the advantages of the lowest possible equipment cost and greatly simplified fixturing. At prototype debug, this may be all that is required or practical. Even when the ultimate goal is full I/O access, a requirement for MCM or board-level test, a TAP-only test is a good starting point. After the TAP-only test is operating, you can add I/O coverage, as shown in Figure 3. In addition, as described in the following section, the TAP-only test can be reused once the unit is installed into the next assembly level.

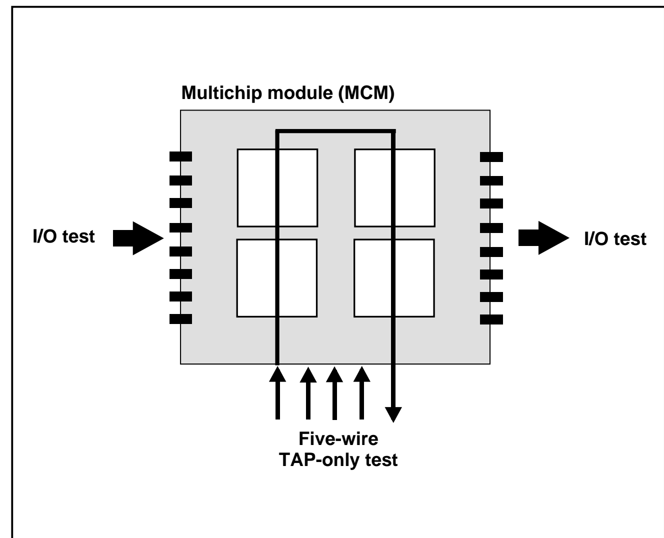


**Figure 3. TAP-only test plus full I/O test**

## III. TESTING AT A HIGHER LEVEL.

The most common introduction to hierarchical boundary-scan testing occurs when one or more MCMs are assembled onto a board. In this scenario, each module is equipped with boundary scan as are other components on the board assembly.

Testing moves to the next level of hierarchy when multiple boards are assembled to create a box, and then to the next higher level when multiple boxes are connected to form a system.

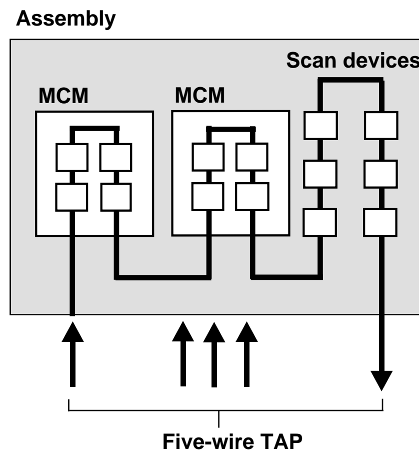


**Figure 4. Simple daisy chain of MCMs and individual boundary-scan devices**

At the board level, it is common to simply daisy chain the devices of each MCM and individual boundary-scan devices on the board into one long chain, as shown in Figure 4. Although the scan path may then seem quite long, 1149.1 allows any devices not involved in a particular test to be placed in BYPASS mode to minimize the overall length of the path.

After the TAP-only tests have verified the structural integrity of the MCMs and the other scan devices, two areas of the board remain untested:

- the I/O pins of the board.
- the interconnects between the MCMs and the other boundary-scan devices.

New patterns have to be developed for these two areas. The TAP-only approach may be sufficient to apply the patterns, or you may need to use some ATE channels to test the off-board I/O connections. In any case, the new TAP-only test can be combined with earlier TAP-only tests (used at the previous level to test MCM and device internals) and reused at the next level of assembly.

As you progress up the assembly hierarchy, the same process is repeated at each level. TAP-only tests for the interior of an assembly are reused at the next level, and additional test patterns are generated for the newly introduced interconnections. Only uncommitted I/O connections require additional ATE control and visibility.

## IV. HIERARCHICAL CHAIN MANAGEMENT.

In the the previous example, the scan paths of MCMs and individual boundary-scan devices were daisy-chained together to form a long chain for TAP-only test. This approach works at the board level when all the MCMs and devices are in place when the board is tested. However, if you want to test a board before mounting the MCMs, or if you want to test boards in a partially populated system, you need a flexible way of linking scan elements.

A multidrop bus provides the flexibility to distribute the testability signals across a backplane in such a way that an assembly can be individually addressed through a special interface device. For example, instead of shifting through all the boards in a system to test one board, you address the interface device on the board-under-test and treat that board as if it were the only one there. Unlike a daisy chain, which connects boundary-scan components serially in a scan path, the multidrop bus connects boards in parallel, busing all five TAP signals to each board in the path. Also unlike a daisy chain, the multidrop bus works no matter how the system is populated—with one, several, or all of its boards.

Currently, there are two approaches to forming a multidrop bus for assemblies with 1149.1 devices. At the high end, the IEEE Std 1149.5-1995 serial bus is ideal for systems that require comprehensive test and maintenance. Support for this complex standard, in the form of interface devices and test hardware and software, is developing slowly. In the years to come, it is likely that 1149.5 will become the dominant method for creating highly testable systems [5].

Today, a simpler approach is available, using variations on the 1149.1 standard itself. Proprietary addressing schemes, available within special interface devices allow

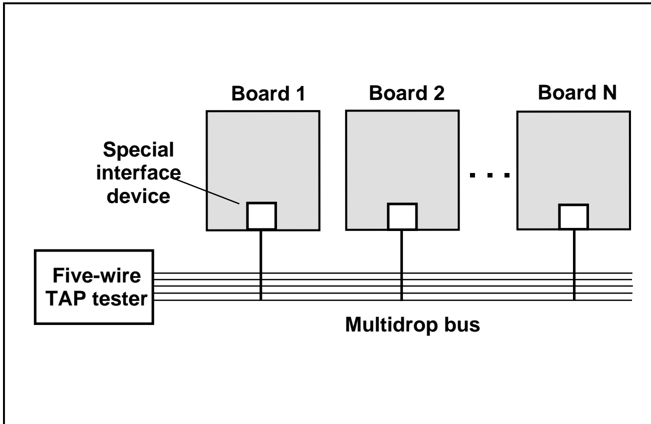


**Figure 5. Connecting multiple boards for box test**

a test program to select an individual assembly for test, and in the process make the bus and the assembly-under-test look like an ordinary 1149.1 bus. This technique, illustrated in Figure 5, has the advantage being well-understood and widely supported [6, 7].

Additionally, some bus interface devices can use dynamically configurable secondary scan paths (SSPs) to support hierarchical test. A board, or higher level of assembly, is connected to a multidrop bus as the test interface to the next higher level. Inside the assembly, dynamic SSPs contain chains of devices that can be included or excluded from the chain, as observed from the backplane, by additional proprietary addressing

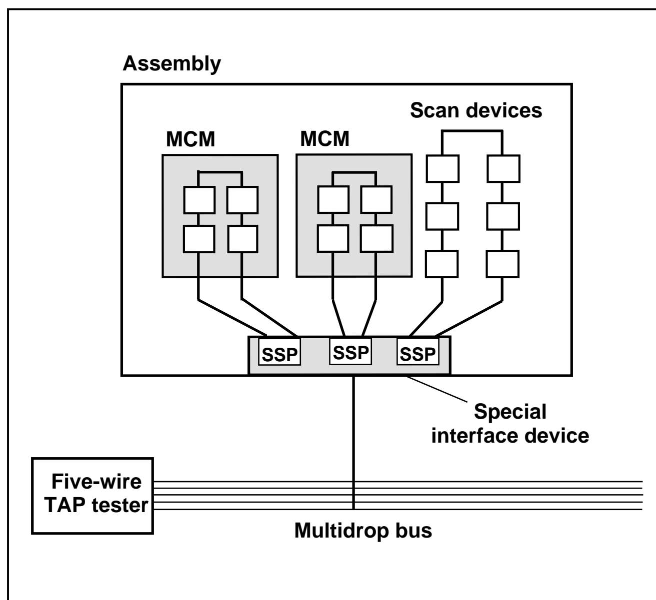


**Figure 6. Using secondary scan paths (SSPs) to support hierarchical testing**

within the interface device. In the example of a board that has two MCMs and a chain of devices (see Figure 6), each MCM can have its own SSP, and the device chain can have its own SSP. Using this approach, any of the devices can be accessed directly from the multidrop bus.

The multidrop bus approach shown in Figure 6 can be extended to support complex hierarchies of assemblies by including interface devices in the SSPs of higher-level interface devices, as illustrated in Figure 7 on the next page. Once addressed, the contents of any SSP in a complex system can be accessed directly from the highest-level multidrop bus.

## V. THE CHALLENGE OF PORTABILITY.

Reuse implies conversion of vectors to various targets, which include simulators, ATE, and embedded test. In order to reuse vectors, it is necessary to express them in a format that can be easily converted to target test environments as needed. Serial Vector Format (SVF) was originally designed as a means of connecting Teradyne's VICTORY software to tools such as the ASSET InterTech Scan-Based Diagnostics system. As part of the ARPA ASEM program for MCM test, Teradyne demonstrated the ability to easily convert from SVF to multiple test targets. SVF is widely used as the exchange mechanism for In-System Programming (ISP) of programmable logic devices that can be configured through the 1149.1 Test Access Port. SVF is being explored as a possible future standard for 1149.1.

Teradyne is supporting broader distribution of SVF through an SVF Converter Kit that is available at no charge from Teradyne's World Wide Web site.

## VI. CONCLUSION.

This paper has explored a test process that reuses test sequences to detect structural faults in the interior of successively higher levels of digital assemblies. However, before tests can be generated at each level, you need a circuit description of the level-under-test.

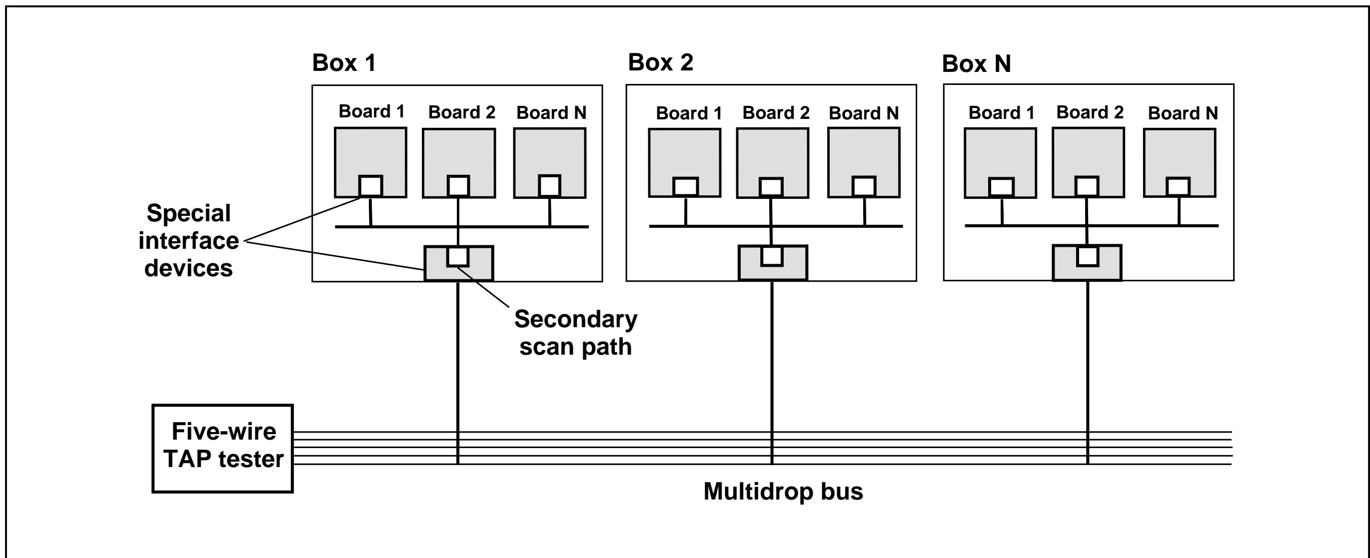


**Figure 7. Connecting scan paths in a multi-level hierarchy**

For unit test of an MCM, you only need to know about the interconnection of the devices within the module. For testing at the board-level, you need a description of each MCM as well as the board-level interconnections. As you continue up the hierarchy to higher levels of system integration, you need to accumulate and reuse all of the underlying circuit descriptions—just as you need to accumulate and reuse test vectors.

The ability to deal with hierarchical circuit descriptions is common in CAE systems. However, board test systems and associated test-generation tools have traditionally taken a single-level view of test, both because of the functional complexity involved and because of the limited use of MCMs. In fact, most board-focused software flattens the circuit description as if MCM boundaries did not exist, or as if each MCM were a big device. For system-level test, tools need to be capable of managing multiple assembly levels using techniques such as hierarchical netlists, hierarchical chain descriptions, and special interface devices.

As manufacturing techniques achieve greater integration at every level—MCM, module, board, box, and system—and test requirements become even more complex, boundary scan will play an important role in reengineering the board test process to support hierarchical test.

REFERENCES.

[1] K. T. Kornegay and K. Roy, “Integrated Test Solutions and Test Economics for MCMs,” *Proceedings of IEEE International Test Conference*, 1995, pp. 193-201.

[2] L. Storey, C. Lapihuska, E. Atwood, and L. Su, “A Test Methodology to Support an ASEM MCM Foundry,” *Proceedings of IEEE International Test Conference*, 1994, pp. 426-435.

[3] P. Hansen, “Taking Advantage of Boundary Scan in Loaded-Board Testing,” *The Test Access Port and Boundary-Scan Architecture* (eds. C. M. Maunder and R. E. Tulloss), IEEE, 1990, p. 81.

[4] G. Wedge, “Using Boundary Scan With a Fault Dictionary To Test and Diagnose Clusters of Non-Scan Logic,” *Proceedings of IEEE Autotestcon*, 1996, in production.

[5] C. Poirier, “IEEE P1149.5 to 1149.1 Data and Protocol Conversion,” *Proceedings of IEEE International Test Conference*, 1993, pp. 527-535.

[6] L. Whetsel, “Hierarchically Accessing 1149.1 Applications in a System Environment, *Proceedings of IEEE International Test Conference*, 1993, pp. 517-526.

[7] J. Andrews, “Roadmap for Extending IEEE 1149.1 for Hierarchical Control of Locally Stored, Standardized Command Set, Test Programs,” *Proceedings of IEEE International Test Conference*, 1994, pp. 300-306.