

# Using Boundary Scan With a Fault Dictionary To Test and Diagnose Clusters of Non-Scan Logic

Gene Wedge

VICTORY Software Development

Teradyne, Inc

Boston, MA 02118

Phone (617) 422-3496 Fax (617) 422-3100 E-Mail: gene.wedge@teradyne.com

**Abstract**—The VICTORY boundary-scan toolset offers fault-dictionary diagnosis of virtual logic clusters, using the diagnostic data provided by a simulator. Using simulation software such as LASAR V6, a test developer can fault simulate the cluster-under-test and produce a fault dictionary in standard LSRTAP format. At run time on a tester, VICTORY's Boundary-Scan Intelligent Diagnostics (BSID) module uses the LSRTAP files as part of its diagnostic database to isolate a reported failure and diagnose the fault. This paper discusses the implementation and requirements of this new capability, which is available for L-Series and Z1800-Series ATE as well as third-party testers.

## I. INTRODUCTION.

Boundary scan gives test engineers the potential to test assemblies for structural faults in circuits that lack physical access to internal nets. Testing and diagnosing the interconnects between boundary-scan devices has become a well-established technology with VICTORY's Boundary In-Circuit Test (BICT) and Virtual Interconnect Test (VIT) products. But ever since the IEEE 1149.1 standard was conceived, boundary scan also has held the promise of using the virtual access points provided by boundary-scan cells to test internal clusters composed of non-scan parts.

In 1994, VICTORY 2.1 introduced Virtual Component and Cluster Test (VCCT) software to generate tests for individual non-scan components or clusters of non-scan components surrounded by boundary-scan logic. Figure

1 illustrates a sample VCCT cluster test scenario. Version 2.2, released in 1995, enhanced VCCT with a cluster definition facility to aid users in carving out the cluster from the larger circuit for simulation and testing. However, the tools still lacked adequate diagnosis of faults internal to a non-scan cluster.

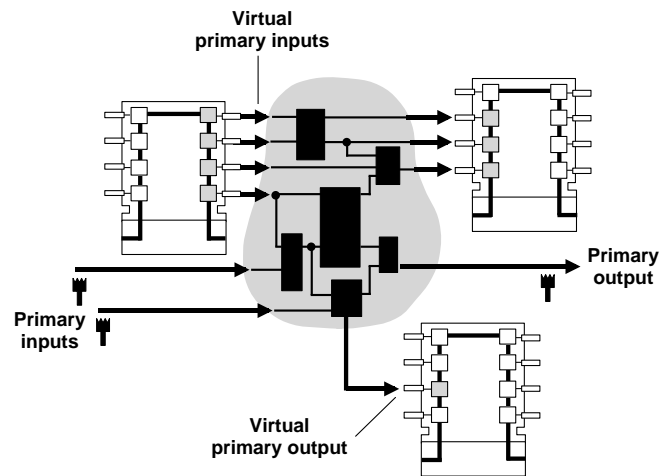


Figure 1. Sample VCCT cluster test scenario

During 1994 and 1995, Teradyne participated in the ARPA ASEM (Application Specific Electronic Module) project. As part of this project, prototype VIT and VCCT diagnostic software was developed for use by VICTORY's Boundary-Scan Intelligent Diagnostics (BSID) module.

As required under the terms of the ASEM program, commercialization of this prototype capability soon

followed with the 2.2 and 2.3 releases of VICTORY software. Version 2.2 introduced diagnostics for VIT testing, providing automatic diagnosis of shorts and opens in nets with boundary-scan access. Version 2.3 added fault-dictionary diagnosis for VCCT cluster testing.

## II. VIRTUAL CLUSTER TEST.

VCCT uses a combination of virtual ATE channels (the scan cells of surrounding boundary-scan devices) and real ATE channels to drive stimulus into and detect response from a cluster of non-scan components. VCCT uses the same technique for virtual component testing of individual non-scan components.

Whether VCCT is used to test a single component or a cluster of components, it is necessary to identify the

primary inputs (PIs) and primary outputs (POs) of the object-under-test. For each individual input, there has to be one boundary-scan lead or tester pin that provides the source of the stimulus within the net, while disabling all others. For each individual output, there has to be at least one boundary-scan lead or tester pin that acts as the measurement point.

For component test, VCCT automatically performs the analysis required to identify the component's stimulus and measurement points, using input files such as the circuit netlist, BSDL models, and the device chain description. For cluster test, VCCT requires an additional piece of information: a description of the cluster's periphery in terms of its PIs and POs. A test developer describes the cluster using a simple cluster definition language, which is based on LASAR's model editing language. Once the cluster is defined, VCCT auto-

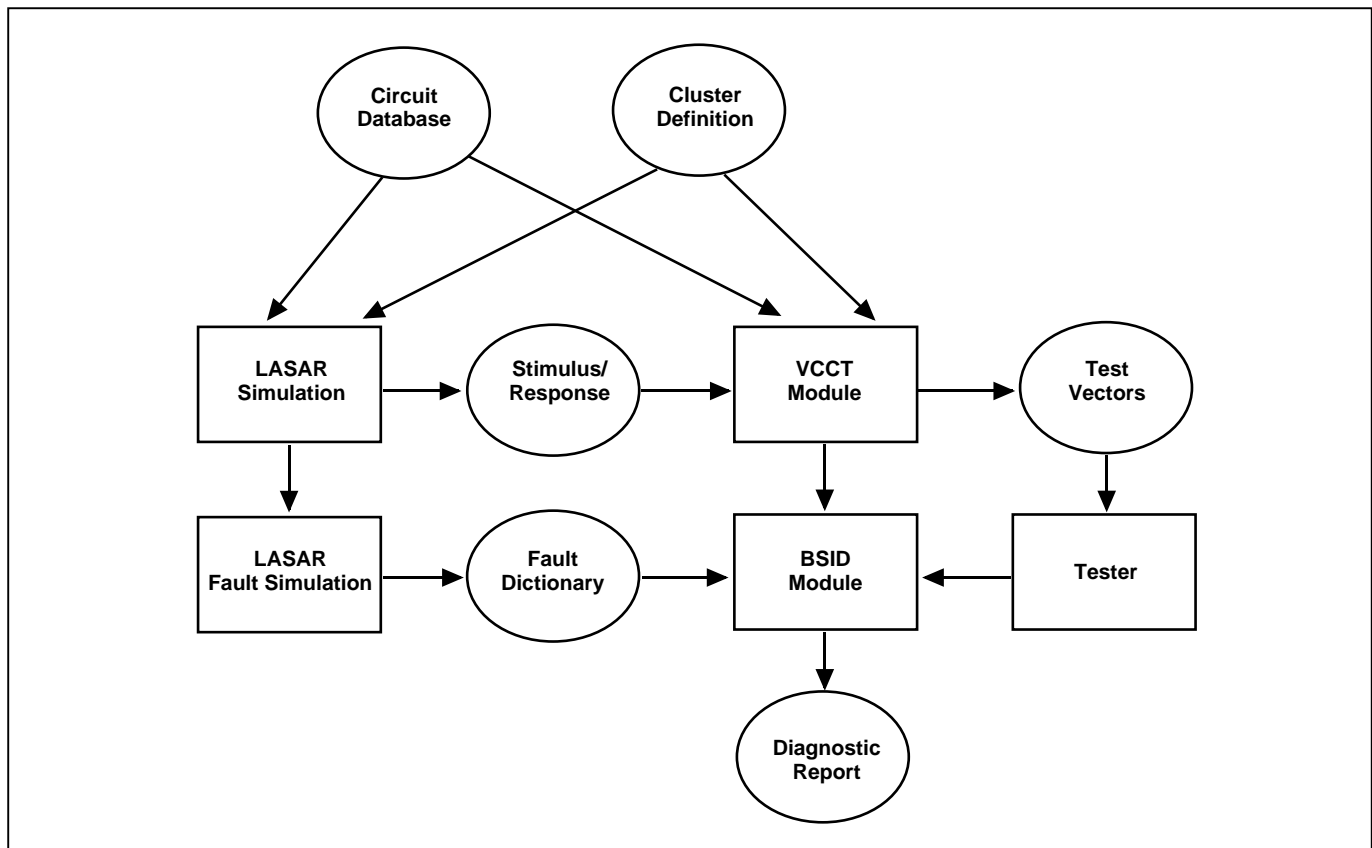


Figure 2. VCCT data flow diagram

matically performs the analysis needed to determine the stimulus point for each input to the cluster and the measurement point for each cluster output.

The ability to use boundary-scan access points greatly simplifies the cluster simulation effort. The simulation software does not need to understand the boundary-scan circuitry in order to simulate the non-scan cluster. It sees the boundary-scan cells, and any relevant tester pins, only as the PIs and POs of the cluster. Timing requirements are relaxed because boundary-scan testing is static. Clusters typically contain small, simply modeled parts since the large, complex, and custom components of a circuit tend to be equipped with boundary scan.

Most importantly, the additional access provided by the boundary-scan logic allows an assembly to be broken up into very small clusters, making it much easier to create thorough stimulus patterns and reducing the time required for simulation and fault simulation.

Boundary-scan access also provides additional diagnostic information, which reduces the likelihood that different faults will produce the same fault signature. This reduction in fault aliasing ensures better fault isolation.

Figure 2 provides an overview of the data flow elements in a VCCT test using LASAR for cluster simulation and fault simulation. VCCT takes parallel stimulus and response patterns from LASAR along with descriptions of the assembly and the cluster, and produces serialized patterns targeted for cluster test. Each of the cluster PIs and POs is automatically mapped either to a tester channel or to a boundary-scan cell.

For each parallel pattern in the LASAR stimulus, VCCT produces a scan vector that loads the appropriate scan cells with data for the virtual PIs and applies the remaining parallel signals through the available tester channels. For response, tester channels receive the parallel signals, and the data for virtual POs are scanned out through the scan chain. The resulting serialized patterns are converted from the standard Serial Vector Format (SVF) produced by VCCT to the

vector format of the target tester and incorporated into the test program for the circuit.

An SVF Vector Converter Kit, which can be downloaded from Teradyne's site on the World Wide Web, supports fast development of translators for a wide range of commercial and DoD-standard automatic test systems.

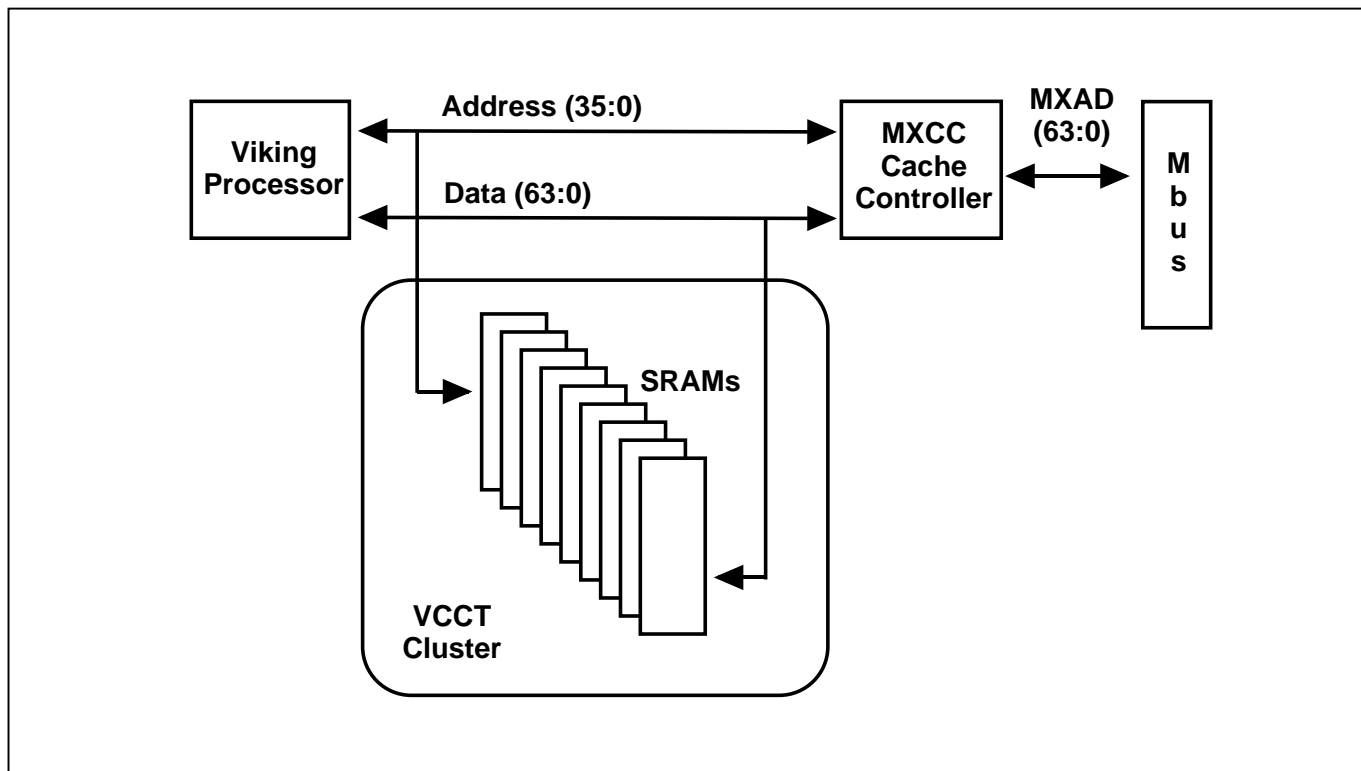
When a failing circuit is detected, the tester reports the failing patterns to the diagnostic engine, BSID, in standard Digital Test Failure Data (DTFD) format. A Failure Reporting Kit is available for converting tester-specific failure data into DTFD.

BSID deserializes the failures detected in the boundary-scan chain, mapping them back to the cluster POs. Combining the failing POs with the failing scan vector number for each failure yields a fault signature. Using a subset of the standard LSRTAP fault-dictionary files and LASAR's well-established search algorithm, BSID looks up the fault signature to accurately diagnose the faulty cluster.

### III. CASE EXAMPLE.

As part of the ASEM project, we were required to demonstrate the prototype software with two test case examples. One was a cluster on a Teradyne board constructed specifically for the purpose of demonstrating the various techniques for boundary-scan test. The other—and more interesting case example—was an MCM, which is described here in more detail.

The MCM incorporated a Viking SPARC processor and an MXCC cache controller, both equipped with boundary scan, plus a bank of eight 128K x 9 SRAM chips with no boundary scan. The memories are nearly completely embedded in the MCM, surrounded by the boundary-scan cells of the CPU and the cache controller. The memory cluster contains 101 nets, only two of which are accessible from the edge of the module. The cluster has 100 PIs and 72 POs. This is a very typical MCM design scenario, in which simply modeled parts such as memories are embedded



**Figure 3. Viking module block diagram**

among large boundary-scan parts. See Figure 3 for a block diagram of the Viking module.

The simulation model for the memories was based on existing memory models, which had to be modified to represent the pipelined architecture of these particular SRAMs. We wrote stimulus patterns by hand, using established memory test techniques targeted at testing external memory connections. We used 84 patterns to fully exercise the address, data, and control lines of the memories. The LASAR fault simulation yielded 98% fault coverage of 1,906 simulated faults. The entire LASAR simulation took about 3 days.

When we ran the VCCT test on a known good module, it passed on the first attempt. We also successfully diagnosed several faulty modules from a limited production run.

#### IV. LIMITATIONS.

The current implementation of the VCCT cluster test process makes use of the L-Series translation features built into LASAR, since this is the most direct path for producing tester patterns that VCCT can use. This path has been easiest to implement, but the steps involve some data that is unique to L-Series ATE. Further work is planned to improve the integration between LASAR and VCCT software, without the restrictions imposed by the L-Series translation.

The VCCT technique places a high premium on the number of parallel patterns used for the cluster test since each parallel pattern involves an entire scan of the boundary-scan chain. For example, for a cluster with a moderate scan chain length of 2,000 cells, it takes roughly 200,000 TCK cycles to apply 100 parallel patterns.

This problem is mitigated by the small size of the typical non-scan cluster, which requires relatively few patterns for thorough structural test.

In addition, the VCCT module performs several optimizations as it serializes the cluster patterns:

- VCCT uses interleaved patterns, providing the inputs to TDI at the same time the responses at TDO are being scanned out from the last scan vector. This effectively cuts the length of the test in half.
- VCCT can take advantage of any compression features the tester has available, such as the PATC WAIT in the L-Series.
- Any scan devices not used in a particular VCCT test is put into BYPASS mode, which can shorten the scan chain substantially. Still, it can be very important to minimize the number of parallel patterns used.

As with any boundary-scan test, the rate at which VCCT patterns can be applied is very much slower than the typical operating speed of the circuit, and the simulation is performed with static vectors. This technique is intended to isolate structural faults, not timing-related problems.

The quality of a VCCT test and diagnosis depends on quality of the simulation. Fault coverage and fault discrimination will depend on the effort put into writing patterns that sufficiently exercise the cluster, while keeping the number of patterns to a minimum. Once again, the task is greatly simplified by the small size of the typical non-scan cluster.

## V. CONCLUSION.

The integration of fault-dictionary capability into VICTORY's boundary-scan diagnostic module completes the framework for productive use of boundary-scan logic to test clusters of non-scan logic, isolate failures, and diagnose faults. This technique is reusable throughout the product life cycle, from design and prototype testing to manufacturing and depot testing of MCMs and printed circuit assemblies. When VCCT is combined with other boundary-scan test techniques, test developers can approach 100% coverage of structural faults in boards that contain a mix of boundary-scan and conventional logic.