

**Frequently Asked Questions
Boundary Scan
New Techniques and Application Practices
w/JTAG Technologies**

Date: July 13, 2005

Q: Which Boundary Scan Vendors are currently supported and can be integrated with Teradyne In-Circuit Testers?

A: Teradyne embraces an open approach to integration. Any third party solution can be supported and integrated with the Teradyne environment.

Q: How are the failure results from Symphony Results Reader passed back to TRACS? Does it require a separate file scanner on TRACS just for the Symphony Results Reader?

A: The Symphony Results are integrated into the standard repair ticket and sent to TRACS for analysis, the same as any other results.

Q: I have been testing boards with 10+ large FPGA's which have pushed the cell count to 40,000 cells. Are there plans to increase the 16,000 cell limitation at ICT?

A: The 16,000 cell limit is a function of limited result memory on the older 228X/TestStation systems. Our new TestStations have 64K of result memory which is normally software limited to 16K for compatibility but can be changed to use the full 64K.

Q: Are there fixturing limitations with boundary scan?

A: You should ensure that you do not probe any internal TDI/TDO connections whilst performing boundary-scan tests that utilize the complete chain because it will cause signal degradation and produce erroneous results. Probing of the boundary-scan control signals should only be done through the primary interface (*i.e.*, access the TDI pin of the first device in the chain and the TDO pin of the last device in the chain, etc.).

Q: The combination of Flying Probe + JTAG means that fewer test points are typically required. Are there tools that allow the user to optimize Test Point assignments?

A: JTAG Technologies provides a boundary-scan fault coverage analysis utility that allows you to assess all of the pure boundary-scan test coverage that is achievable within a particular design. The utility provides a list of nets that are connected to cluster (non boundary-scan) devices. You can either choose to create a boundary-

scan cluster test for a memory device, etc., or assign a test point to these nets to allow physical probing.

The utility creates a report that quantifies the maximum achievable boundary-scan test coverage for a particular design, facilitates the import of APL files created for each boundary-scan test (e.g., interconnect, memory cluster, standard cluster, etc.) and calculates the actual test coverage achieved, so that you can qualify how good your test coverage is against what was ultimately possible.

This analysis can be completed at the schematic capture stage, prior to committing to board layout and specifying where test points should be placed.

Q: Is Teradyne using any particular third party solution internally with the 228X platform?

A: No, we only use our own tools internally for our own boards.

Q: How does this tie into Victory software?

A: Victory still exists as a native boundary scan solution on both the Spectrum and Z1800 test platforms. We support Victory as a viable solution; however we recognize there are solutions better suited for different applications, whether they are in the test environment or design environment. We have no intention to discontinue the support of any solution. Recently, you may have seen press releases around the fact that Teradyne licensed Victory source code to Acculogic to further advance the product.

Q: Is there a preferred method to generate certain tests?

A: Teradyne does not recommend one vendor's solution over others. Preference is typically a decision best based on the customer's application and test environment.

Q: I have several cases of needing RC components on the TCK line due to unreliable (intermittent) results. Do you know of others who have this problem, or is it a fixture problem?

A: JTAG Technologies' boundary-scan DFT guidelines recommend the TCK signal be terminated on the board with an AC termination using a 68-ohm resistor in series with 100-pf capacitor to GND. This will reduce the level of overshoot and undershoot at the receiving devices and prevent double-clocking, etc.

Q: Should I always integrate ICT with Boundary-scan? If my boundary-scan test is long or CPLD/FLASH programming is long compared to analog or basic ICT, isn't the ICT resource not being used well? (i.e., it's just a power-supply during that time).

A: Integration depends on a number of factors. We would not suggest tying up a ICT system for a long series of boundary scan tests. It only makes sense if you can

improve the defect detection by adding tests at ICT which have negligible impact on test time.

Q: When testing boards with no access to the pins of the device, but there is access to the TAP pins, does this scenario have a solution to keep at ICT and not create a second test center (*i.e.*, desktop or functional).

A: Although there may not be physical access to boundary-scan device I/O pins, it may still be possible to test non-boundary-scan devices connected to these pins, providing there is either a library model to describe the cluster devices or the primary input and resultant primary output patterns are known (*e.g.*, truth table) to allow a cluster test to be created.