



Avoiding Damage to Low Voltage Devices During In-Circuit Test

Tony Suto July 2006

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Assembly Test Division

Agenda

- Re-cap WPI experimental findings
- Highlight key IC device damage mechanisms
- Describe how damage mechanisms can occur during conventional in-circuit testing
- Steps that can be taken to mitigate these potentially damaging scenarios
- Summary



WPI Research Project

- An independent study to identify the potential mechanisms that can damage modern low-voltage CMOS devices and understand their relationship to electrical testing
- EOS due to electrical testing was examined and an experiment was conducted using pulsed voltage waveforms to emulate typical conditions encountered during in-circuit electrical testing
- Attempt to correlate experimental results between amplitude and duration of the voltage pulse waveform and device degradation due to one or more failure mechanisms



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Science and Technology.
And Life..

WPI Conclusions

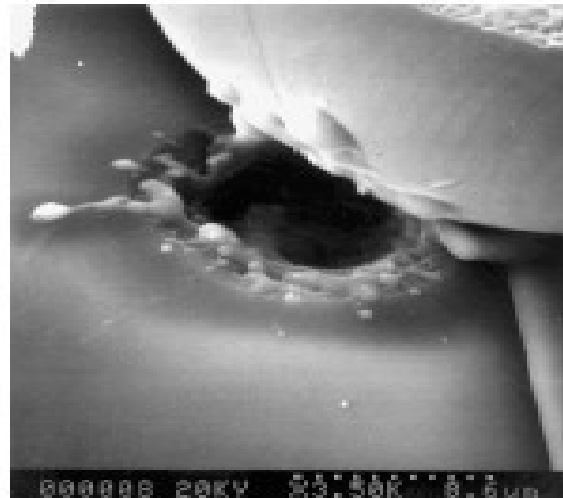
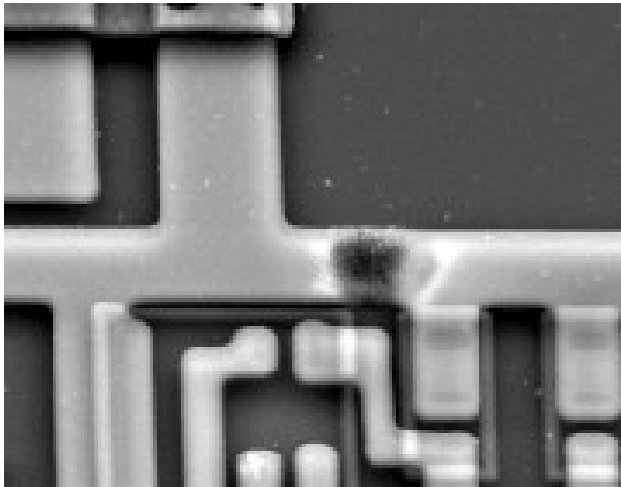
- Low-voltage digital logic devices are sensitive to damage during electrical test due to shrinking feature size
- Providing adequate ESD protection is difficult without compromising the speed and performance aspects of the device
- Caution must be observed when testing IC devices with thin oxide technologies
- When developing test programs, test engineers should be aware that stress due to transient over-voltage conditions is possible in electrical test systems
- Experimental results show that the anode hole injection or '1/E' model is a good tool to predict the safe stress limits tolerated as a function of over-voltage pulse amplitude and duration
- View the study: www.teradyne.com/atd/resource/type/web_recordings.html

Investigation of Device Damage Due to Electrical Testing. Rosa Croughwell and John McNeill, WPI, 2006

Summary: Low voltage devices can be more easily damaged at ICT

Over-Voltage Failure Modes

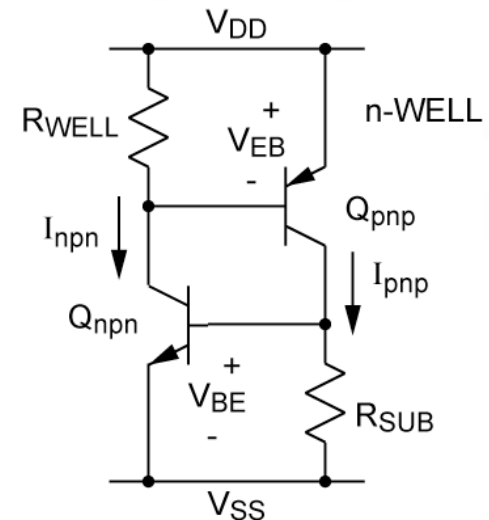
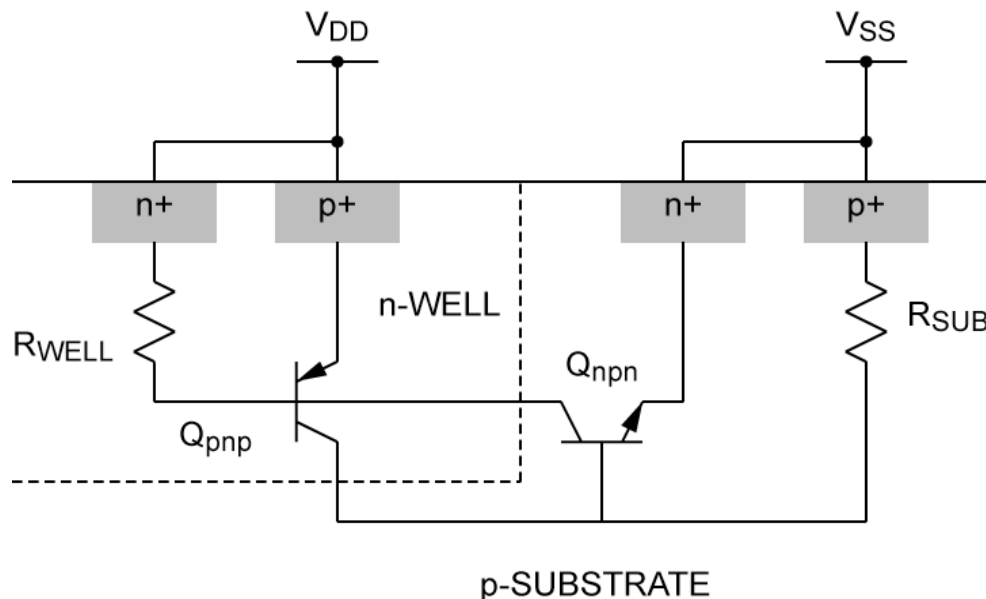
- ESD protection diode damage
 - Caused by applying $>V_{dd}$ (+0.7 Volts), or V_{ss} (-0.7 Volts) to IC pins
 - Reverse biased ESD junctions can avalanche and fail
 - Forward biased ESD diodes can thermally fail
 - Metal to or from protection circuits can fail from Joule heating
 - Stressed ESD protection devices may allow the device to prematurely fail in the field



Over-Voltage Failure Modes

- CMOS Latch-Up Damage

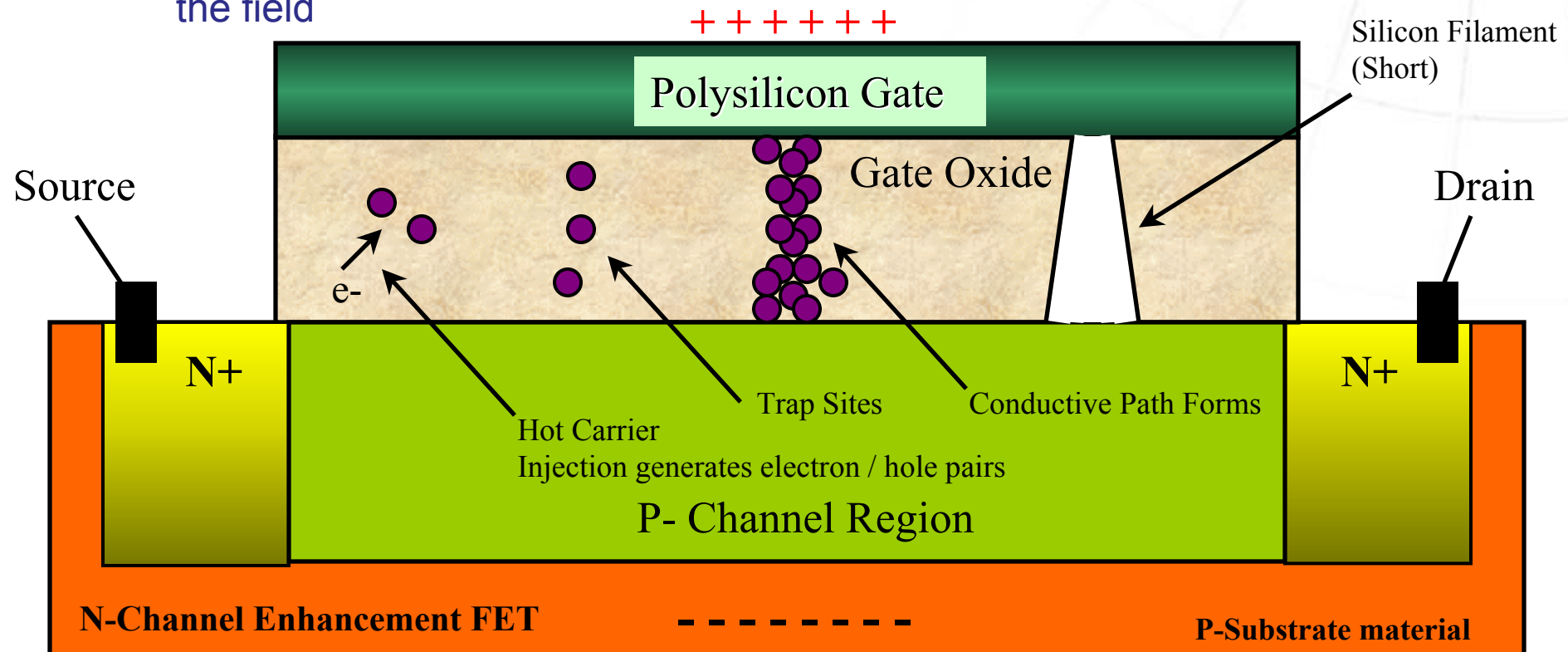
- Initiated by a transient over-voltage condition on I/O pins ($V_{CC} + 0.7V$), or ($V_{DD} - 0.7V$) or greater
- Can cause an over-current condition, catastrophic damage
- Large currents I_{npn} and I_{pnp} flow and form a low-impedance path across the supply terminals
- Thermal damage often occurs due to large resulting currents



Over-Voltage Failure Modes

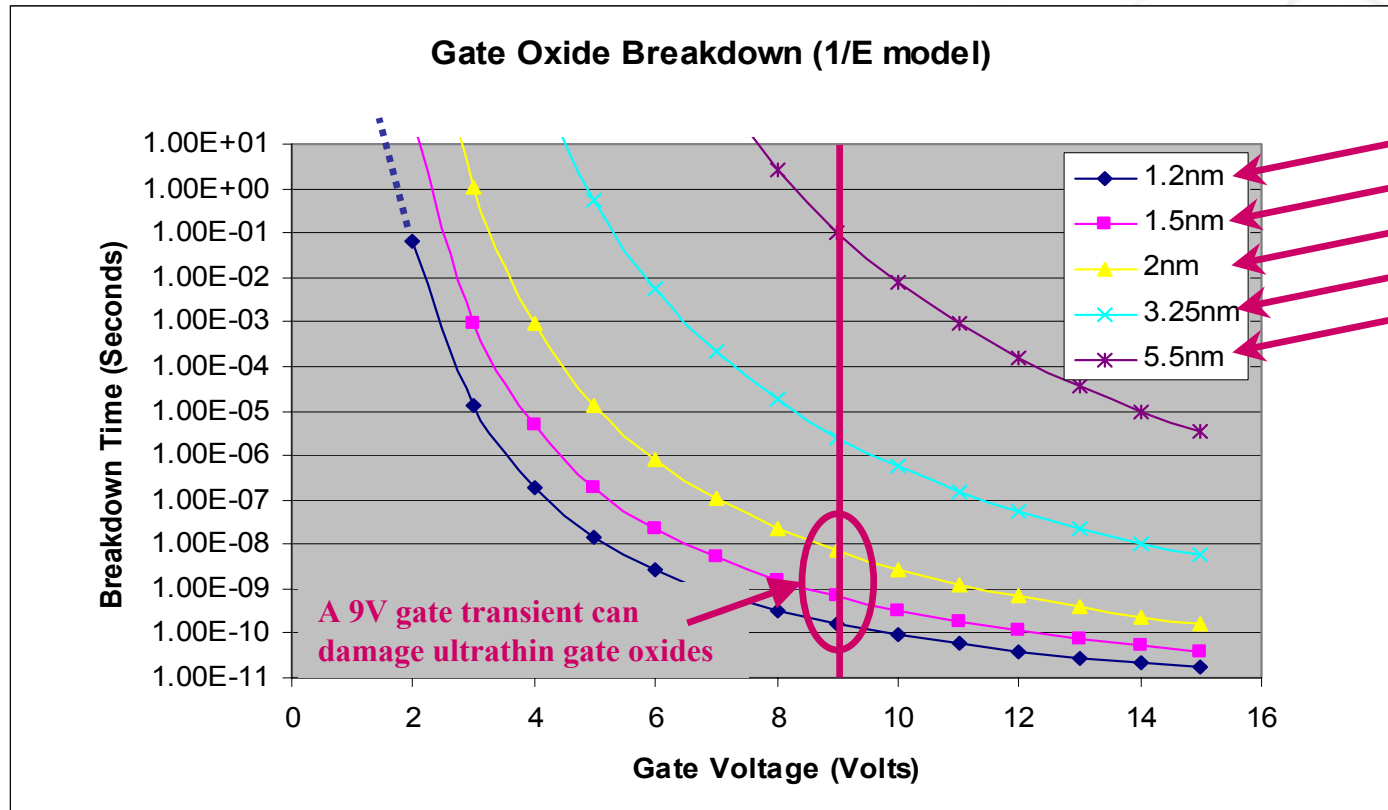
- FET transistor gate oxide damage

- Fet input of output transistor gate oxide can be “punched through” by large over voltage condition
- Time dependent dielectric breakdown (TDDDB) can cause device failures in the field



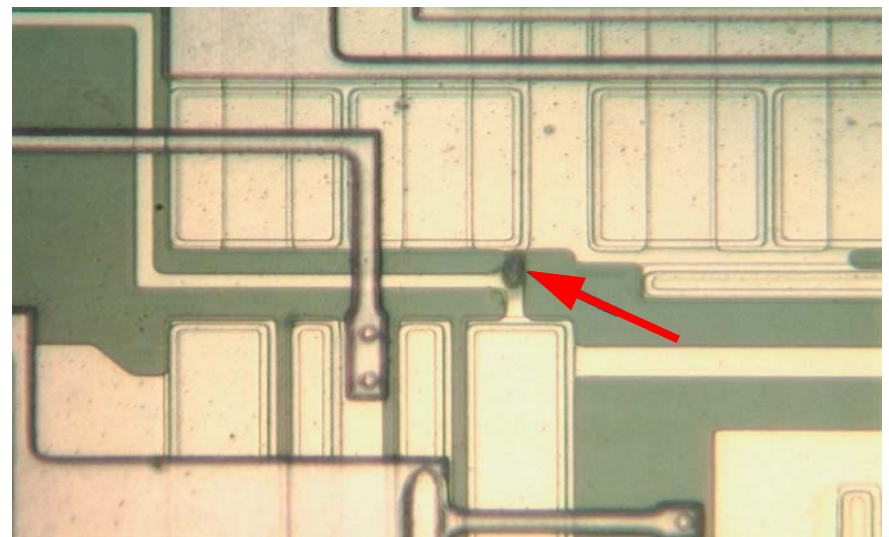
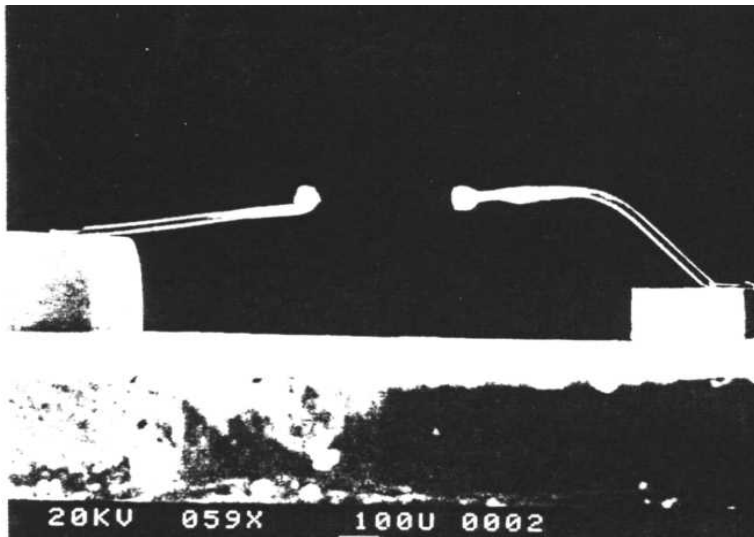
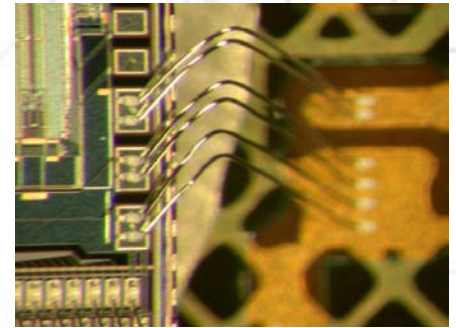
Gate Oxide “1/E” TDDDB Breakdown Model

- $T_{bd} = C1 * EXP(C2/E_{ox})$, $C1=5.58E-13, C2=4.25E8$



Joule Heating Induced Failures

- Well understood in the industry, backdrive induced
 - UK MOD DEF 00-53 / Issue 2.
- Violation of current density design rules in metal, or bond wires, beyond adiabatic limits
 - Conductors can deform, weaken, or fuse
 - Key factors include total chip backdrive current and time



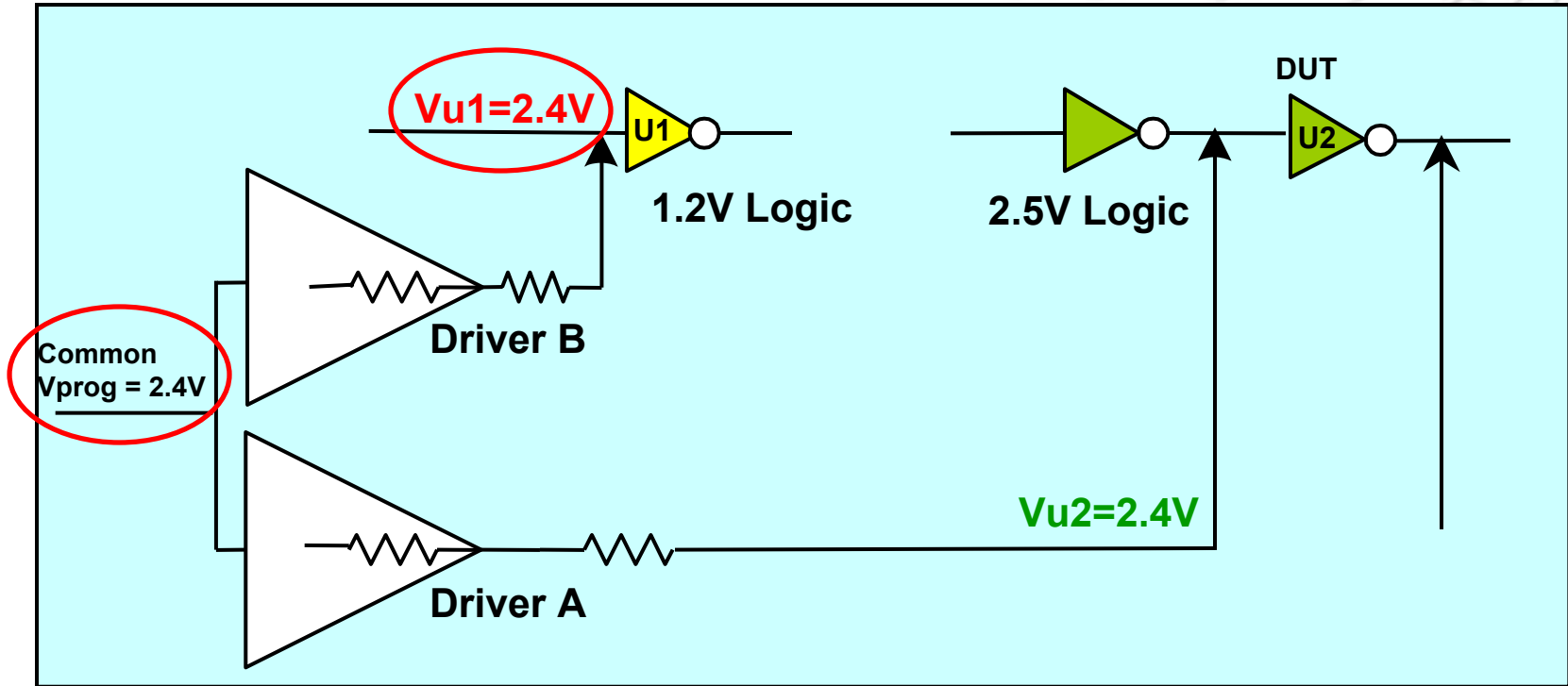


Device Damage During ICT and Mitigation Strategies

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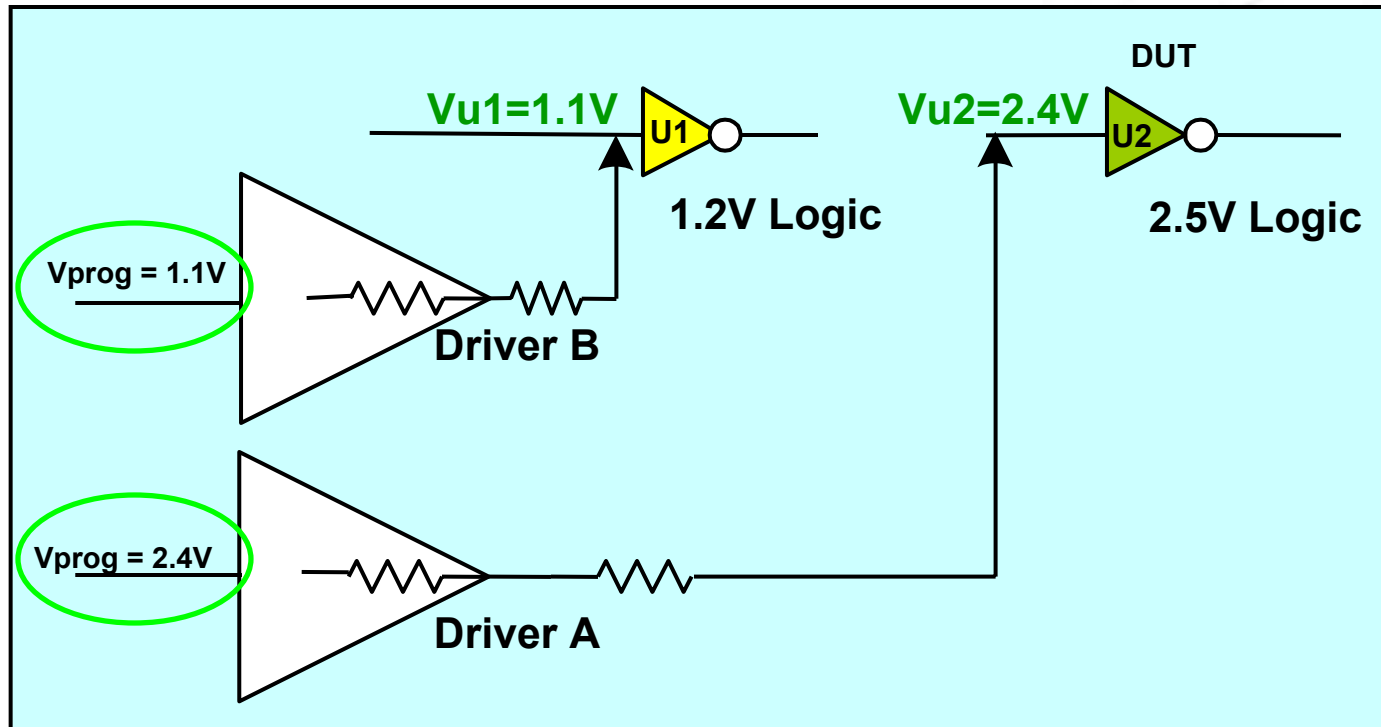
Over-Voltage Stress During ICT: Shared Logic Level Assignments



- Conventional testers use group or shared logic level assignments
- Driver A and B are forced to use the same logic level assignments
- Satisfying voltage requirements for U2 causes U1 to be exposed to over-voltage condition and possible damage

Shared logic assignments can damage IC devices

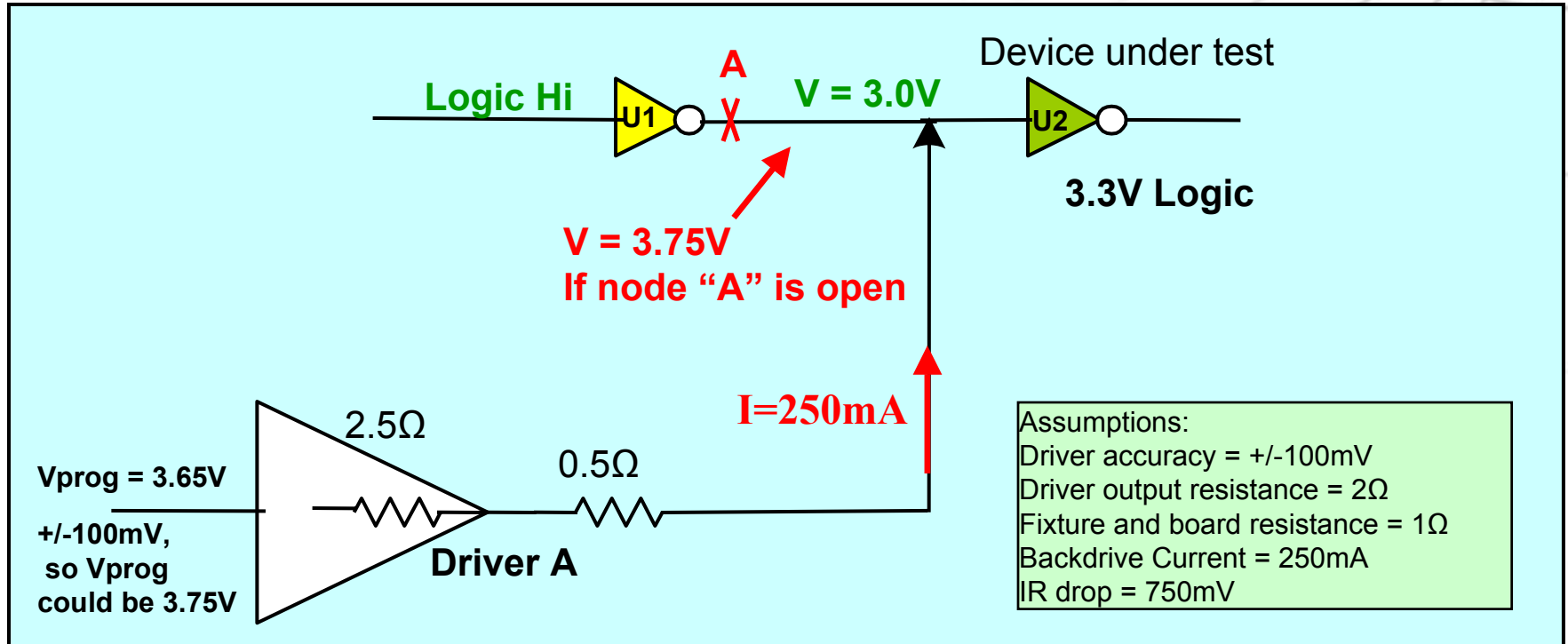
Over-Voltage Stress Eliminated with Per-Pin Logic Level Assignments



- Testers designed for low voltage technologies use independent logic levels
- Driver A is programmed to apply 2.4V and Driver B is programmed to apply 1.1V

Devices are tested within their safe operating regions

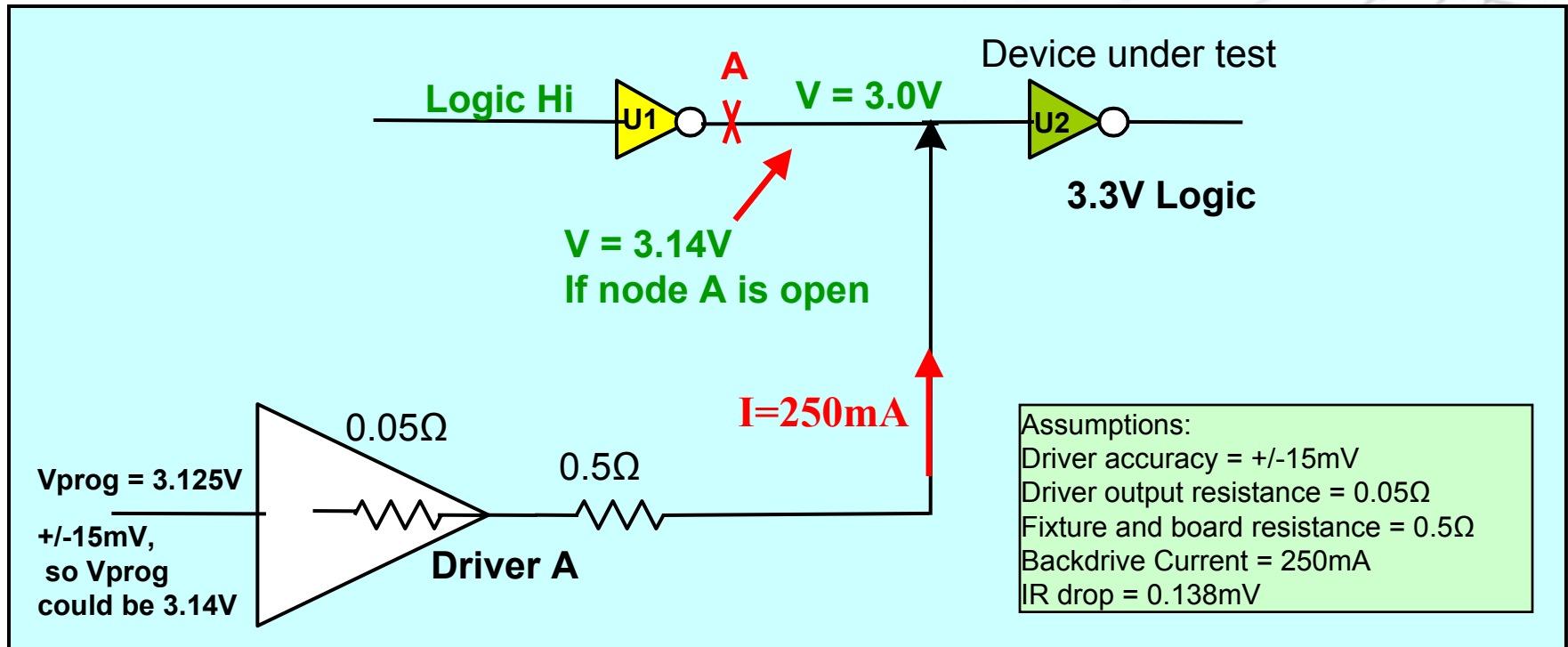
Inaccurate, High Impedance Drivers Can Cause Over-Voltage Stress



- Driver A must be programmed above 3.3V to accommodate backdrive IR drops.
- An open on the output of U1 forces an over voltage condition on the input of U2

U2 can experience over voltage stress, from open pin!

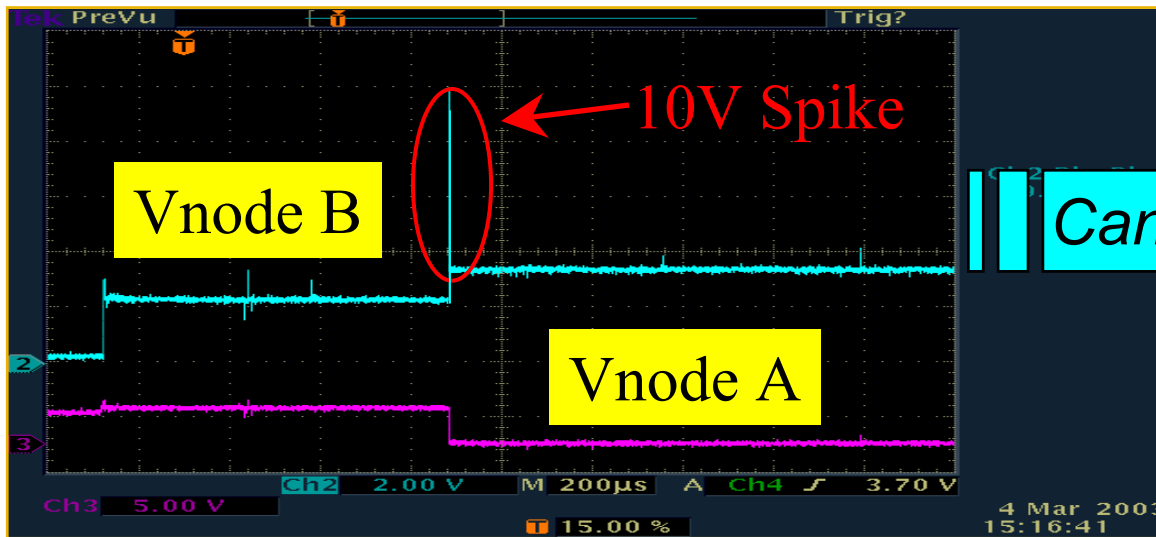
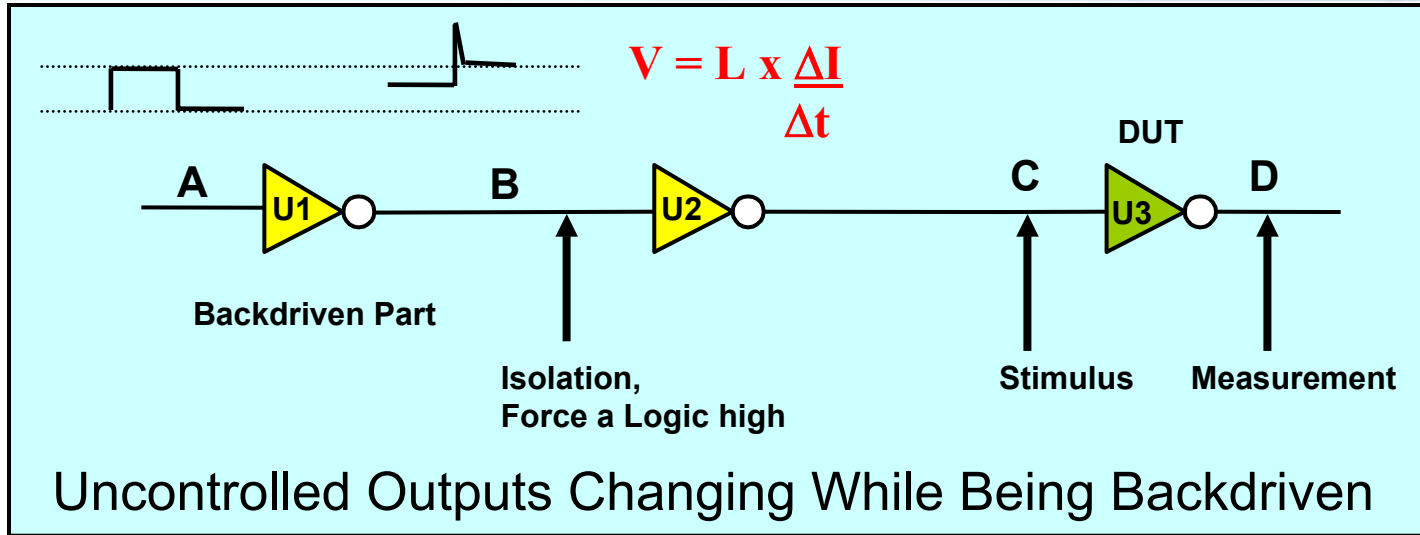
Accurate, Low Impedance Drivers Help to Eliminate Over-Voltage Stress



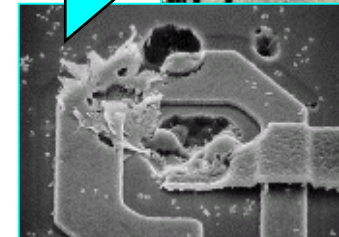
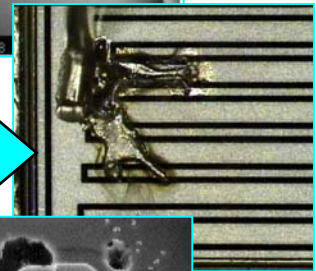
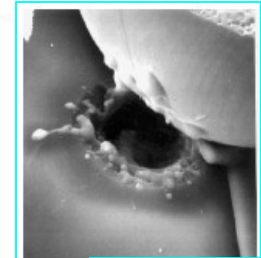
- Driver A can be programmed below 3.3V to accommodate backdrive IR drops.
- An open on the output of U1 forces a safe voltage of 3.14V

U2 has safe voltage applied, even with open U1 pin

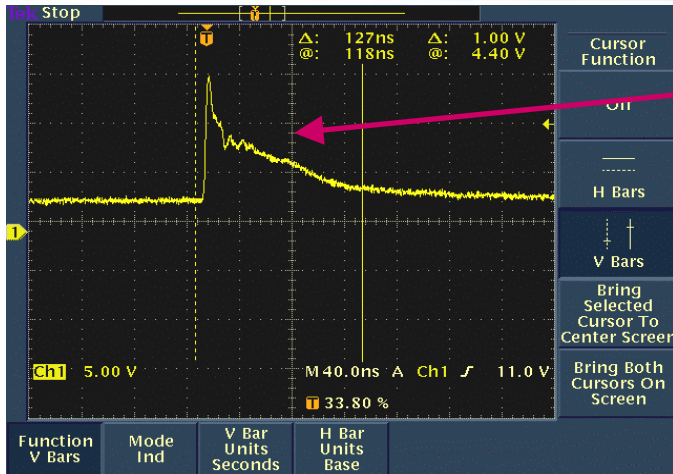
Over-Voltage Stress Caused by Inadequate Isolation Algorithms



Can lead to



Poor Isolation Can Damage Digital Parts

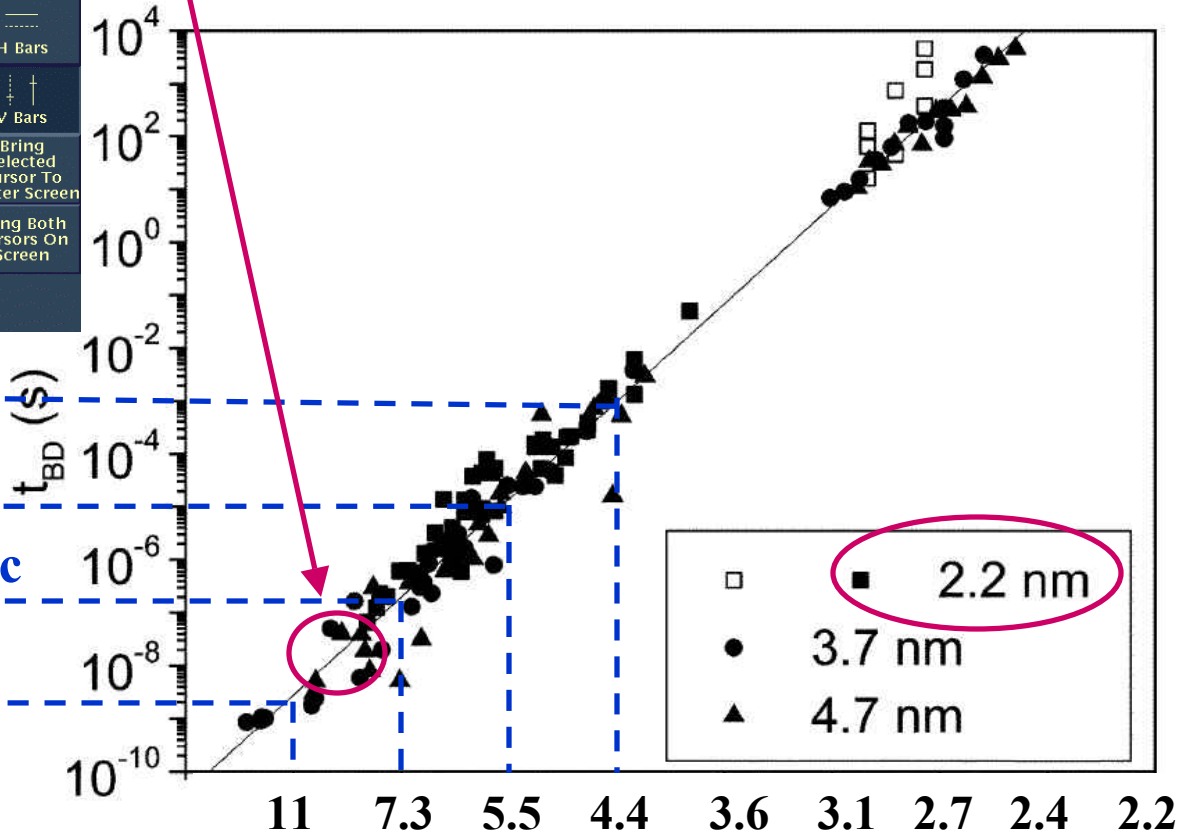


9V backdrive spike for 40nsec, 16V peak for 10ns !

74LVT240A 3.3V.
Backdriven high then
Tri-stated.

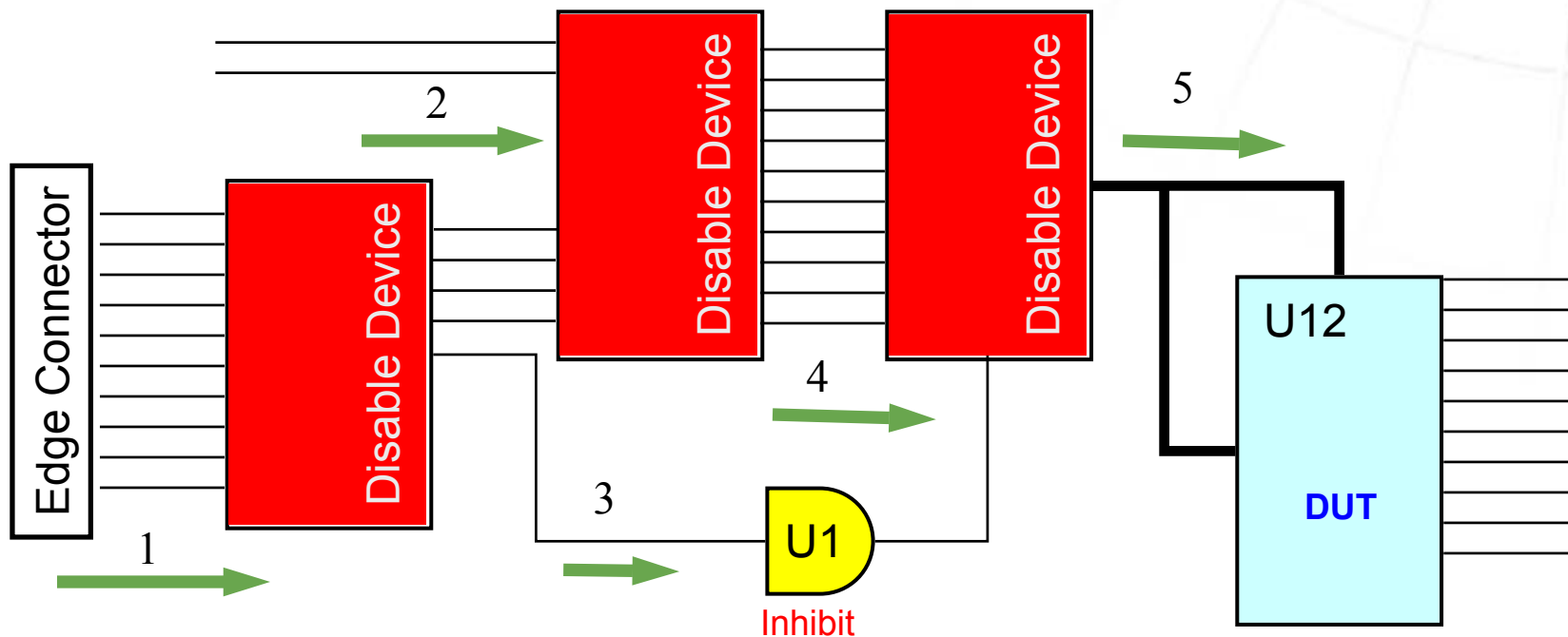
Time to Failure (sec)

1msec
10usec
200nsec
2nsec

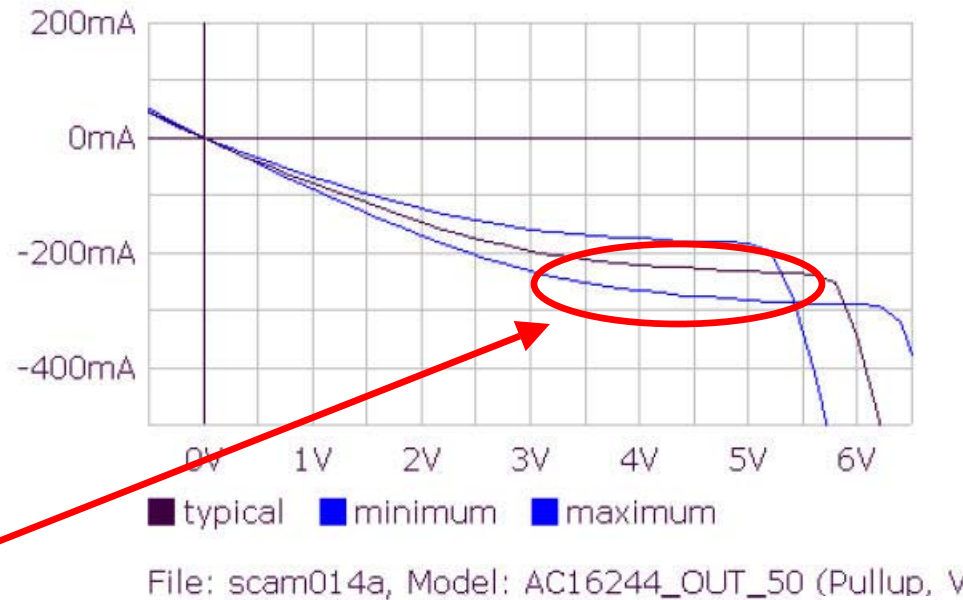
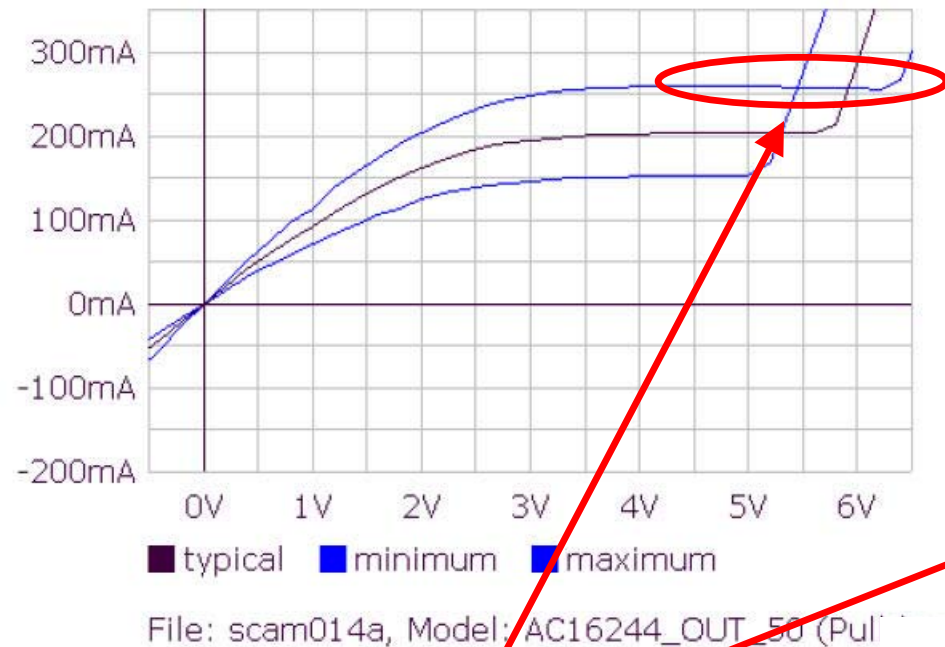


MLDI Isolation Software Eliminates Voltage Transients

- Multi-Level Digital Isolation Software
 - Prevents voltage transients caused by unsuppressed digital changes/feedback caused by on-board activity
 - Sequence of isolation is critical to eliminate transients



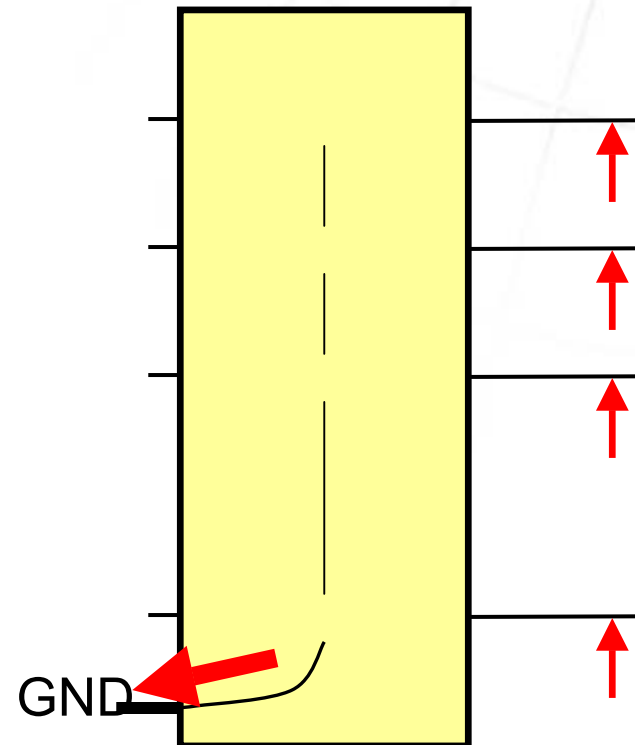
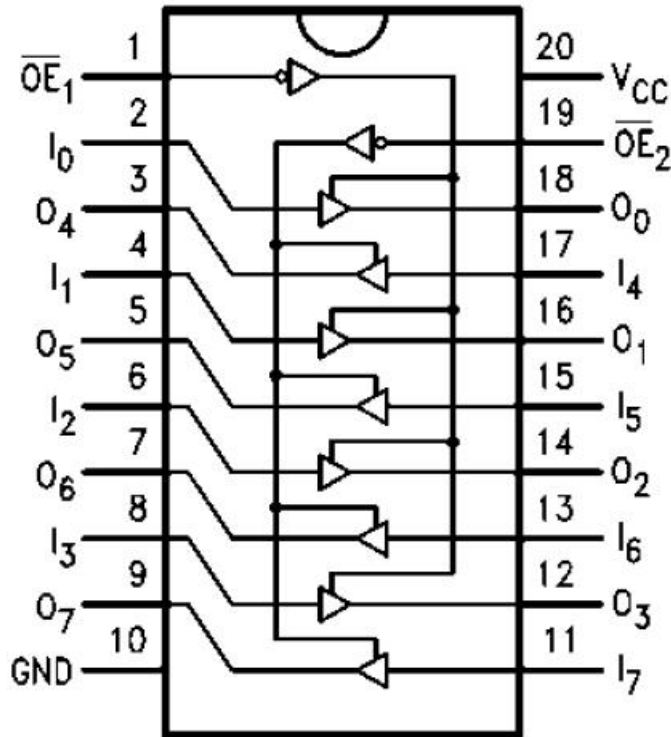
Over-Current Stress: BackDrive Plots 74AC244 Family



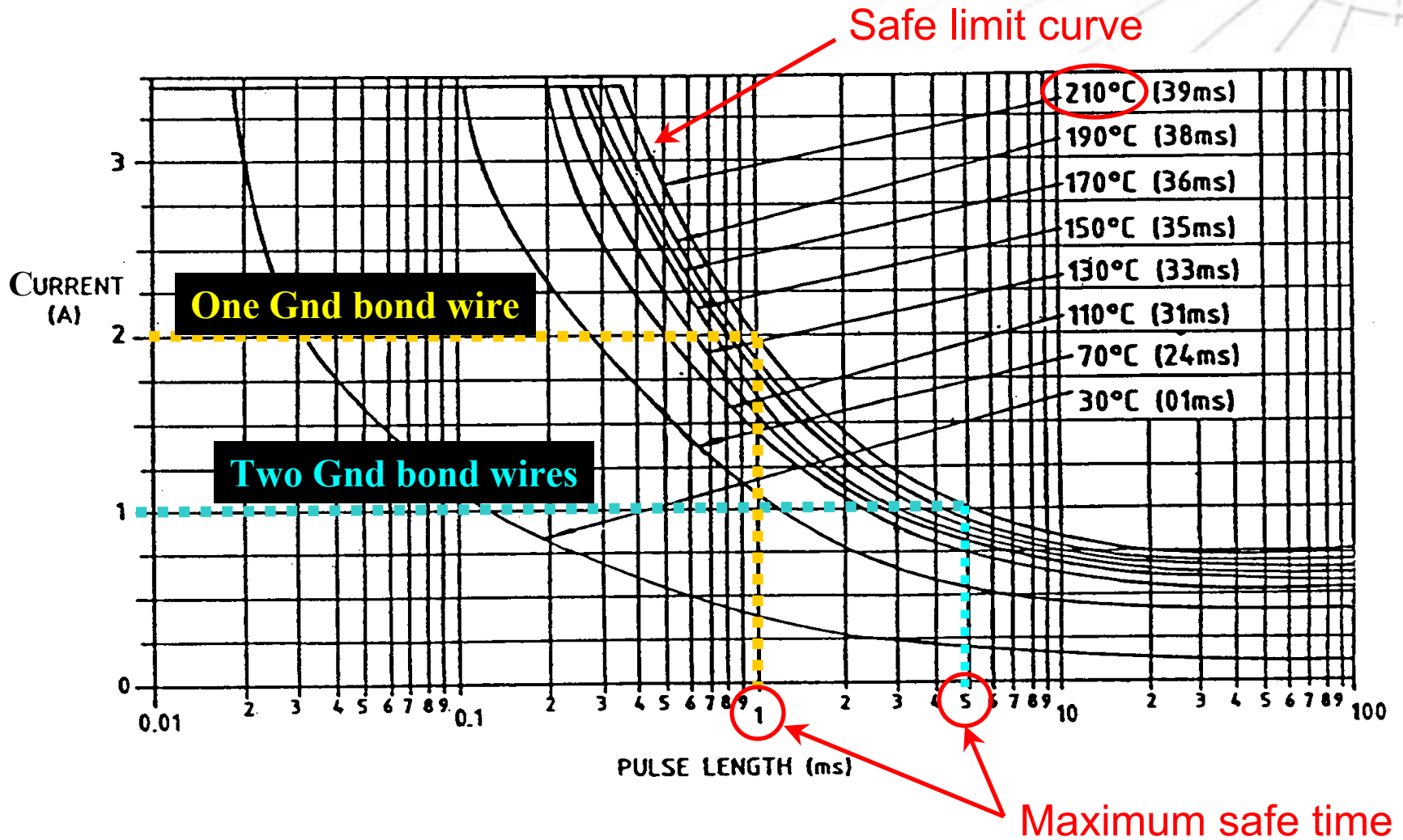
Backdrive current can approach 250mA or more,
even on modern IC parts

Over-Current Stress: BackDriving 74AC244

- Worst case: backdrive entire bus driver IC.....all the backdrive current flows through single ground connection and associated bond wire(s)



Backdrive Current / Pulse Length in 1 Mil Diameter Aluminum Bondwire



No Visibility into Backdrive Events When Using Conventional ICT

- Backdrive Analysis Report Summary: PC Motherboard
 - Digital Bursts with Backdrive Conditions: **17 of 17**
 - Number of Backdrive Events greater than 50mA: **217**
 - Number of Nets Exposed to Backdrive Conditions: **96**
 - Number of Nets Backdriven multiple times: **28**
 - Maximum Backdrive Current: **543mA**
 - Average Backdrive Current: **131mA**
 - Median Backdrive Current: **87mA**
 - Longest Backdrive Duration: **258ms**

Customer claimed that test program was fully debugged and that there was no backdriving on this board!

Some Reasons for Uncontrolled Backdrive Events

- Inadequate digital isolation vectors during digital testing
- Incorrect programming of drive levels that exceed device input compliance and accidentally turn on ESD structures
- Bi-directional output bus drivers were connected to pin drivers before chips were switched to input mode
- Accidental backdriving of discrete small-value resistors that are connected between digital devices
- Wrong code loaded into programmable devices

Real-Time Backdrive Current Measurement and Control for ATE Driver

Capabilities that measure and control backdrive currents and duration in real time, on a per-pin basis

Debug Environment

DEVICE LABEL: U33_B1: (NAND tree Test)
DEVICE NAME: U33
DEVICE TYPE: 82801 (I/O Controller Hub - 3V)

PIN	NODE	NAIL	BACKDRIVE
A3	PICH_HLCOMP	106	79.06 mA
G1	LAN_RXD1	640	73.79 mA
R21	RSMRST_	90	131.76 mA
W11	PCLK_ICH	105	84.33 mA
Y20	OVCUR_1	147	469.08 mA
R22	FERR	614	76.42 mA
C12	CPUINIT_	743	450.64 mA
D11	SB_A20M_	575	563.95 mA
Y17	SUS_STAT	531	73.79 mA
	GGNT_	61	171.29 mA
	RBF_	67	237.18 mA
	SBA0	122	176.56 mA

- Program safe limits for IC devices
- Identifies and eliminates excessive backdrive currents that can stress IC components
- Identifies faults that are not normally detected
 - Wrong program in PLD
 - Open or Faulty Enable Pins
 - Incorrect Isolation Vectors

Backdrive Failure

Device: U33

Type: 82801

Pin: R22

Net: CPUINIT_

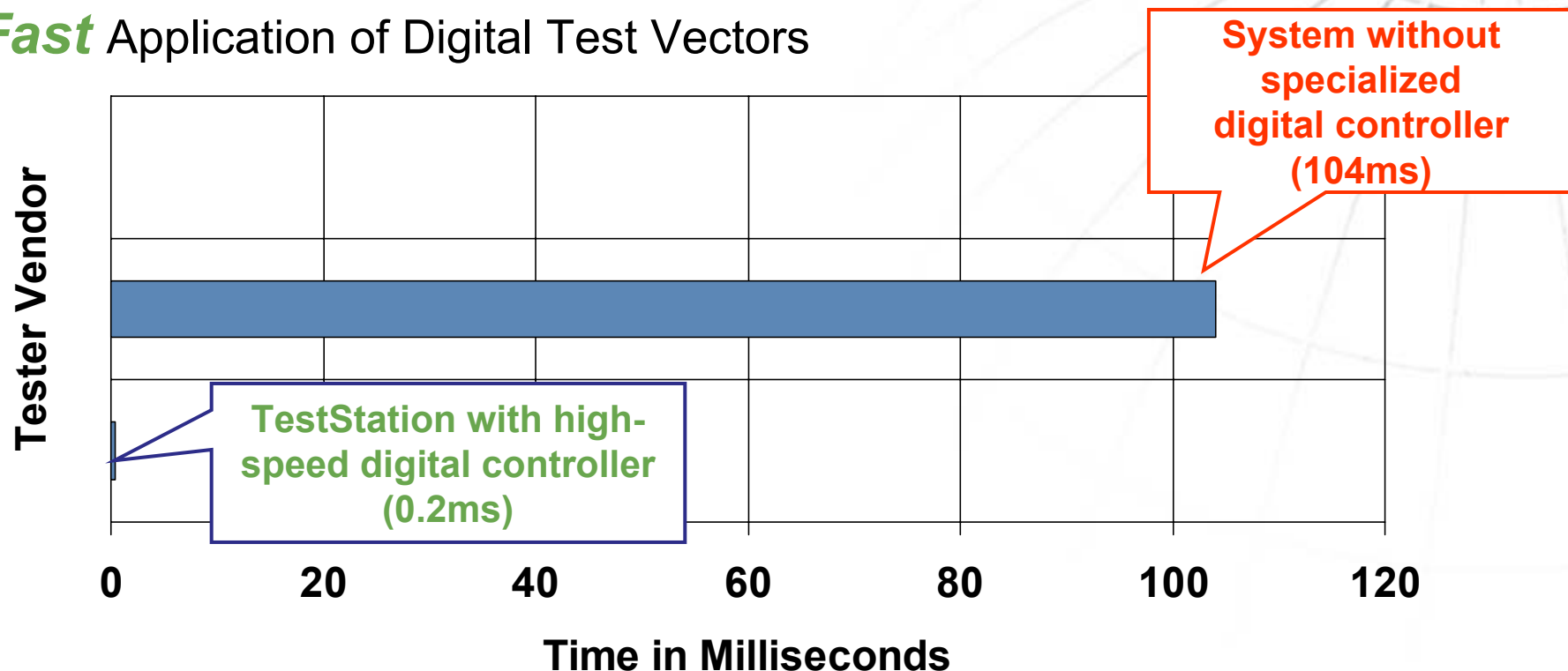
Exceeded Backdrive Current Limit of 100mA

Production

Environment

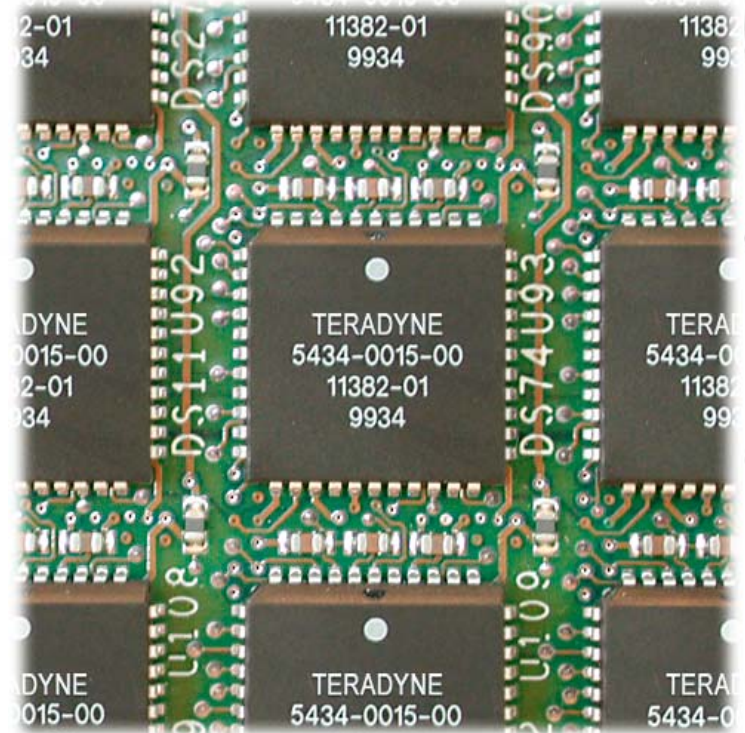
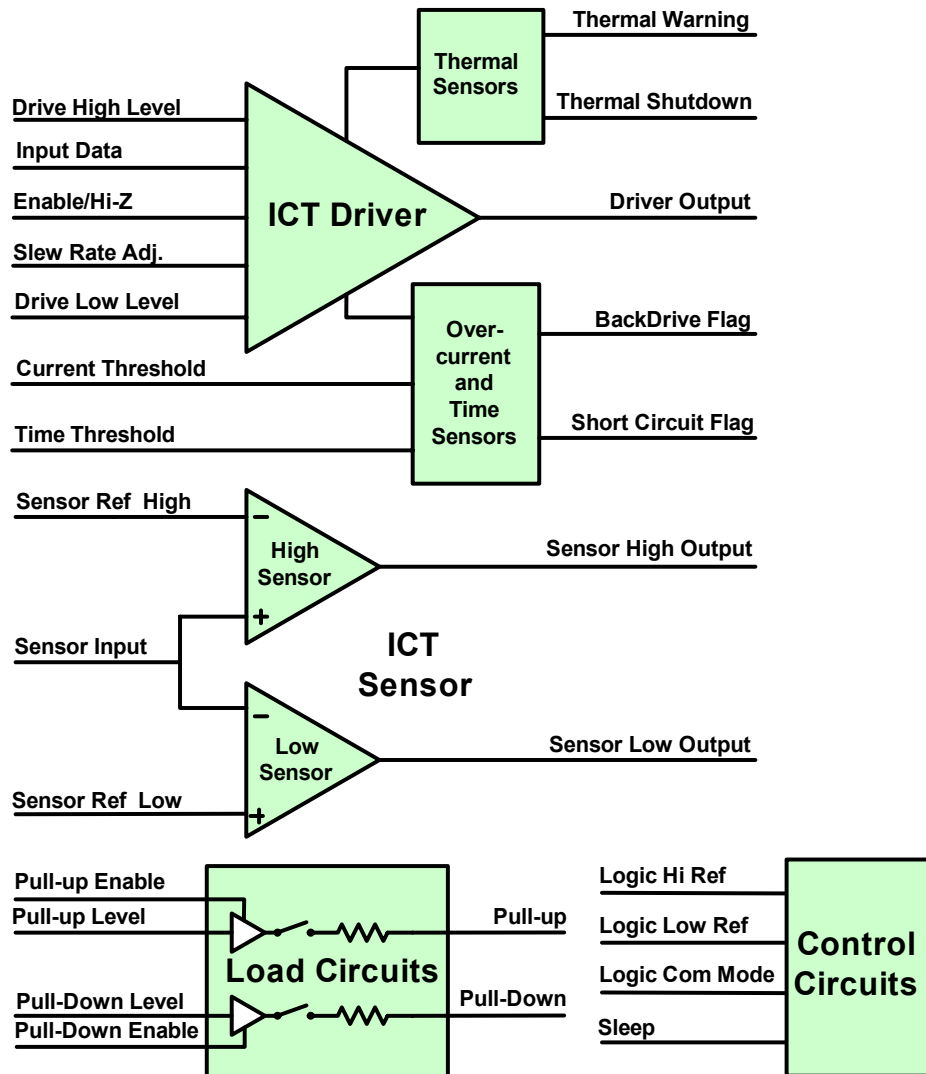
Dedicated High Speed Controller Minimizes Over-Current Stress Time

Fast Application of Digital Test Vectors



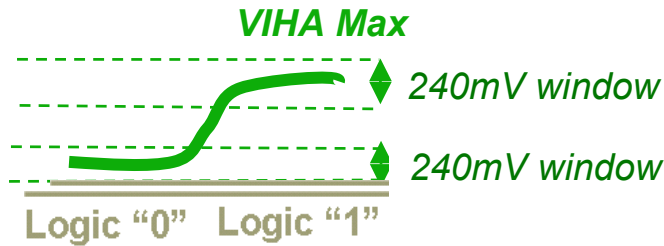
- Vectors applied over 500 times faster than testers without specialized controller
- Significantly shortens backdrive duration
- Reduces likelihood of device damage from Joule heating

Anatomy of Teradyne Pin Technology



- Low output impedance, closed-loop driver
- Integrated, real-time backdrive detection
- User-programmable backdrive amplitude and duration
- Dual threshold sensor
- Programmable load circuits
- Driver output monitoring

Teradyne's TestStation ICT platforms: Designed for low voltage testing

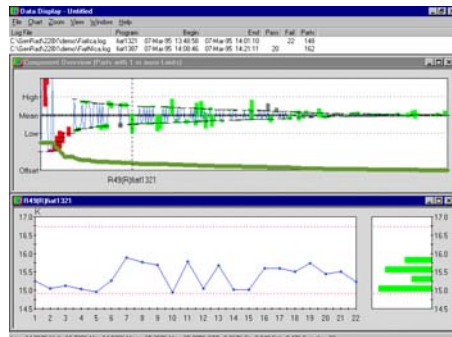
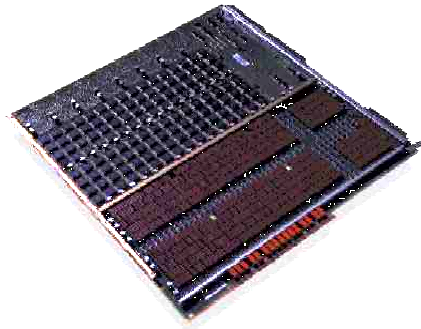


- **Highest Accuracy**

- Accurate driver and sensor voltage
 - +/- 15mV
- Pin-programmable voltage settings
 - Eliminates shared logic families

Comprehensive DUT Protection

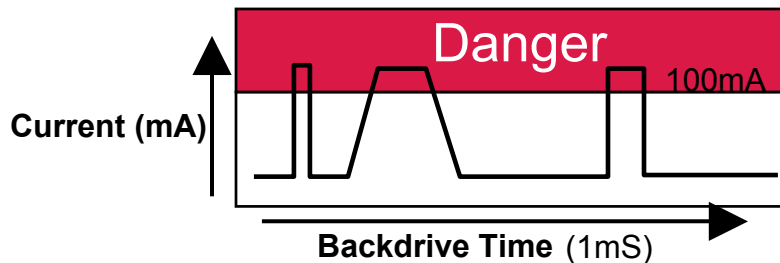
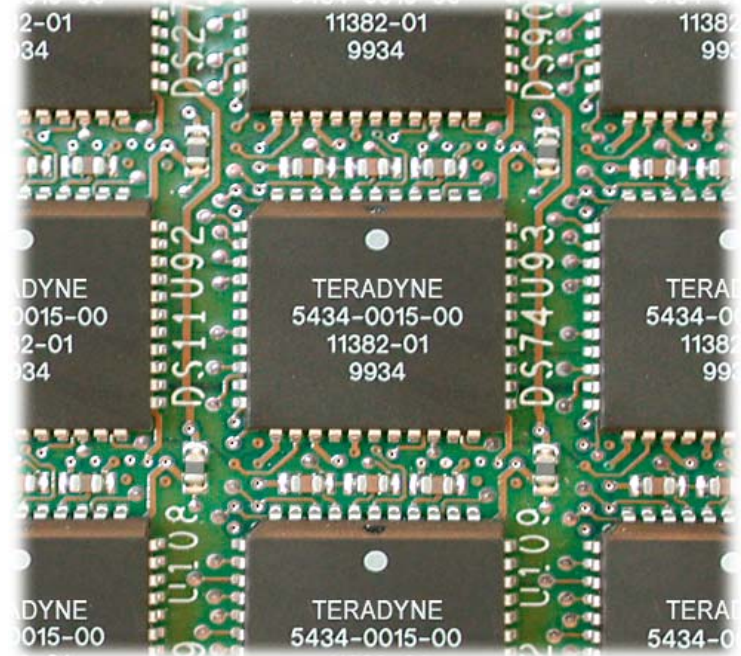
- Real-time current measurement
 - Prevents backdrive damage
 - Identifies incorrect logic families, wrong part
- Backdrive limits for current and time to limit power used while backdriving
- High-speed digital controller to minimize backdrive time
- MLDI software minimizes backdriving and voltage transients
- Saves \$\$\$ in scrap, rework and field repairs




SafeTest™ Industry Awards and Recognitions



- Recognized as Innovative New Product
 - APEX 2004 Innovative Technology Showcase
- “Best in Test” Nomination and Honorable Mention
 - *Test and Measurement World* 2004 Best in Test competition
- Protected under US Patent Law
 - Only Teradyne testers have real-time backdrive current measurement and control capabilities



 US006114848A	
United States Patent [19] Suto et al.	[11] Patent Number: 6,114,848 [45] Date of Patent: Sep. 5, 2000
[54] DIRECT-MEASUREMENT PROVISION OF SAFE BACKDRIVE LEVELS	
FOREIGN PATENT DOCUMENTS 0415319A2 6/1991 European Pat. Off. G06F 11/22	
[75] Inventors: Anthony J. Suto , Sterling; Robert J. Muller , Westford; John D. Montz , Fall River, all of Mass.	
[73] Assignee: GenRad, Inc. , Westford, Mass.	
[57] ABSTRACT	
[21] Appl. No.: 09/231,001	
[22] Filed: Jan. 14, 1999	
Pin-driver circuitry in each of an automatic circuit tester (10)'s digital driver/sensor circuits (36) includes a current	

Summary:

- Device damage **can happen** during electrical test
- In-circuit systems that test low voltage devices need to:
 - Have tight control of voltage drive levels
 - Monitor and backdrive control current levels
 - Minimize current stress duration
 - Eliminate transient over-voltage conditions



References

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- [8] Elyse Rosenbaum, Leonard F. Register, "Mechanism of Stress-Induced Leakage Current in MOS Capacitors", IEEE Trans on Electron Devices, vol. 44, no 2, February 1997
- [9] Jianlin Wei, Lingfeng Mao, Mingzhen Xu and Changhua Tan, "The Experimental Investigation on Stress-Induced Leakage Current Under Fowler-Nordheim Constant Voltage Stress", Inst. Of Microelectronics, Peking University
- [10] Jie Wu and Elyse Rosenbaum, "Gate Oxide Reliability Under ESD-Like Pulse Stress," IEEE Trans on Electron Devices, vol.51, no 9, September, 2004
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- [13] Ministry of Defence, "Safe Operating Limits for Backdriving", Defence Standard, 00-52/Issue 2, July 2, 1999
- [14] Texas Instruments SN74AUC16420 Data Sheet (SCES390E – March 2002 – Revised December 2002).
Copyright 2006, Texas Instruments Incorporated.
- [15] Investigation of Device Damage Due to Electrical Testing. Rosa Croughwell and John McNeill, Worcester Polytechnic Institute



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