

Welcome to the Teradyne Web Seminar

**“Designing Test Strategies for
Modern PCB Assembly”**



TERADYNE



Founded 1960
NYSE: TER
2001 Revenue: \$1.4 B

- 8,000 employees
- 50 locations in 20 countries
- www.teradyne.com
- Headquarters: Boston, MA



The slide features a blue background with a faint world map. It includes several small images: a white test chamber, a person working at a computer, a large industrial test system, a computer monitor, a large industrial test system with a computer, and a close-up of a circuit board. The Teradyne logo is prominently displayed at the bottom.

This web seminar is presented by Teradyne's Assembly Test Division. With over 40 years of innovation, Teradyne designs and manufactures hardware and software test solutions for electronic products ranging from components to systems to entire communications networks. Headquartered in Boston, Teradyne's 8,000 employees worldwide in 20 countries are helping the world's most successful technology companies maintain their competitive advantage in a global market.

Your Presenter



Amit Verma
Product Marketing Engineer
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Your presenter today is Mr. Amit Verma, Product Marketing Engineer for Teradyne's Assembly Test Division. Mr. Verma chairs the National Electronics Manufacturing Initiative (NEMI) "test strategy" project and participates in the "DPMO" project. Both NEMI projects have broad participation from leading professionals in the electronics manufacturing industry. Prior to joining Teradyne, Amit played a major role in designing test strategies and purchasing ATE hardware at a leading EMS company.

Please note Amit's email address. You may wish to contact him with questions or comments.

Agenda

- What technology trends will affect the way your products are tested?
- What ATE hardware is right for your products?
- How can test strategies help you gain competitive advantage?
- What tools are available from Teradyne to help you design best-in-class test strategies?
- Questions and Answers

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These are the topics we'll cover and questions we will attempt to answer for you in today's presentation.

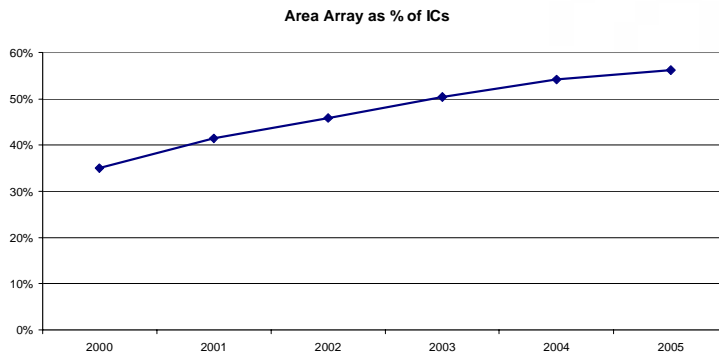
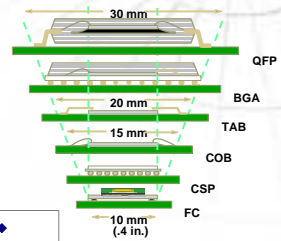
What Technology Trends Will Affect The Way Your Products Are Tested?

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Technology Driver – Loss of Visual Access

- Changing package geometries are reducing the fault coverage of human visual inspection techniques
- By 2005, 55% of all multi-led ICs will use area array packaging



Source:
Electronics Trend
Publications Inc.
April 2002

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QFP – Quad flat pack, bga – ball grid array, tab – tape automated bonding, cob – chip on board, csp – chip scale package, fc – flip chip

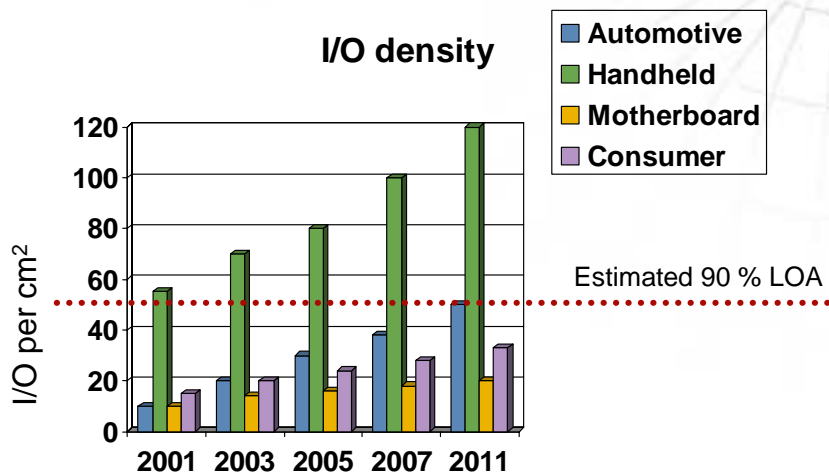
The density and sheer number of interconnections on many of today's circuit boards is beyond the ability of human inspectors. New packaging technologies like BGA and the requirement for RF shielding also pose obvious problems for human inspectors.

The chart shows 55% of all ICs will have hidden joints by 2005.

As solder joints become more difficult to inspect, the inconsistent application of subjective visual inspection criteria is also of concern.

Reduced access and inconsistent results means reduced fault coverage, necessitating alternate methods of inspection like AOI and AXI.

Technology Driver – Pin Density Driving Loss of ICT Access



Source : NEMI 2002 Roadmap Report

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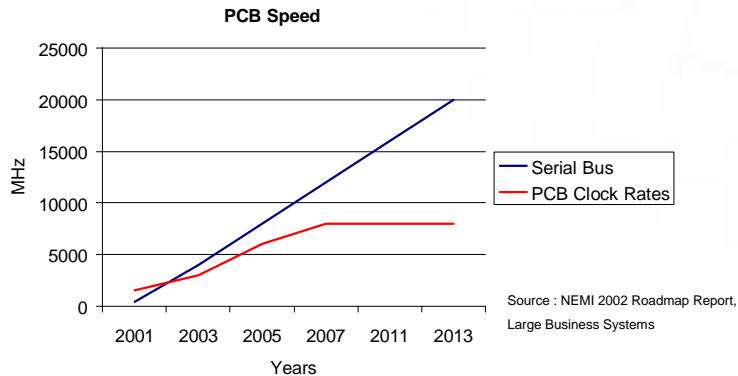
The increasing density of interconnections is making physical access for bed of nails testing more constrained due to limited board real-estate for in-circuit test pads.

This chart estimates up to 90% loss of access at 50 IO/cm². The handheld product segment surpassed this benchmark in 2001.

As trends toward reduced access continue, manufacturers are losing ICT fault coverage, which increases interest in alternate test methods like imaging.

Technology Driver - Loss of ICT Access at High Frequency

- The placement of electrical test points can have a negative impact on signal integrity at high frequencies



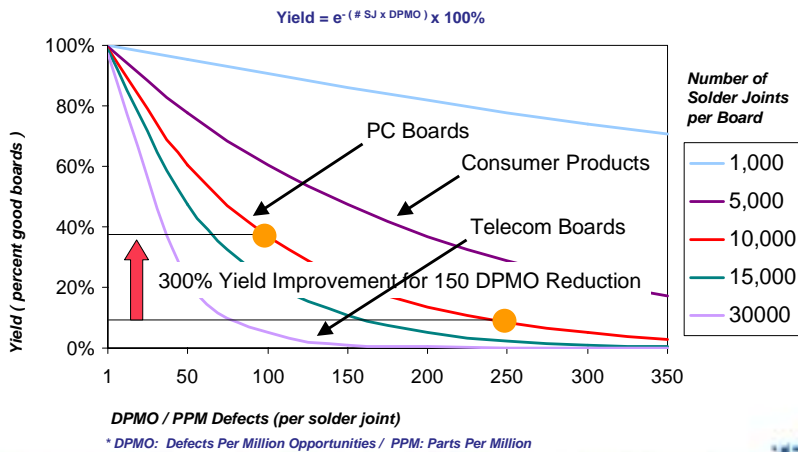
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Physical space constraints on circuit boards are only one dimension of the access problem.

Higher frequencies demand controlled impedance interconnects with minimum discontinuities; these are limiting test access even when physical size is not a design constraint.

Technology Driver - Increasing Board Complexity

As the number of solder joints per board increases, so does the potential for faults → thereby increasing the need for both test coverage and process improvement.



As the number of solder joints per board increases, so does the potential for faults → thereby increasing the need for both test coverage and process improvement.

It is not uncommon to find circuit boards with solder joint counts that exceed 10,000.

Concurrently, assembly process complexity is driving high structural DPMO rates because boards often undergo numerous assembly stages – all this is leading to declining yields.

The chart shows the trend toward declining yields for boards of different solder joint counts at varying DPMO rates. [animate 3]

We can see a board with 10K solder joints is guaranteed single digit yields at DPMOs above 250. [animate 1]

We also see an opportunity for 300% yield improvement if a manufacturer can reduce DPMO rates from 250 to 100.

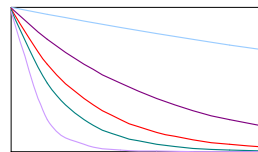
For this reason, there is an increased focus by manufacturers reduce DPMO rates and find defects closer to source to counter a cycle of ever-declining yields. Because the vast majority of faults are structural, imaging methods are most capable of finding defects sooner in the process and providing measurement data for process improvement and DPMO reduction.

Not part of script: It is important to note that the chart represents mathematically calculated yield from an inspection machine with 100% structural defect coverage.

Technology Drivers – Introduction of Lead Free Processes

- The introduction of lead free solder will change many manufacturing variables
- Current human visual inspection criteria will become obsolete
- Manufacturing processes will require rapid ramp-up / re-tuning

NOTE: Both AOI and AXI are capable of inspecting lead free joints.



Need for Process
Improvement

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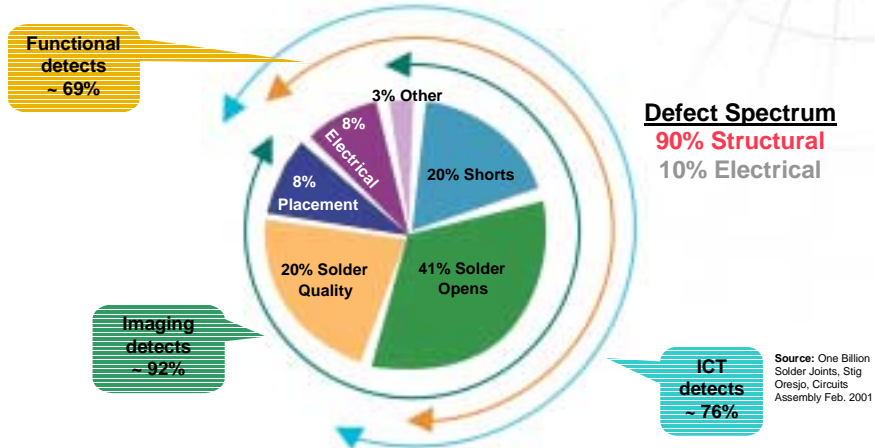
The introduction of lead-free solder is on the horizon for manufacturers worldwide. These new materials and assembly methods will inevitably have a negative impact on process yields as engineers struggle to cope with change and find a new “equilibrium” for their manufacturing processes. It has taken 2 decades of continuous learning to achieve the quality performance levels we have with eutectic solder; manufacturers will be under pressure to achieve those same levels of quality in weeks with the introduction of lead-free solder. The scope of re-optimization that will need to be completed is truly immense.

Those manufacturers that have process measurement solutions like automated inspection will be at an advantage to control the negative impacts of this and other manufacturing process changes.

Because many lead free joints are not “shiny”, visual criteria like IPC610 will need to be re-evaluated and perhaps rendered obsolete, also increasing interest in imaging inspection methods.

Technology Driver - *The Defect Spectrum*

No single test technology provides coverage for the entire fault spectrum (sample defect spectrum shown)



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Manufacturers are recognizing that up to 90% of all defects are structural, not electrical in nature. This trend is causing engineers to consider imaging methods that are well suited to detecting structural failures, as part of their broader electrical test strategy.

The data in this particular chart is from a study by Stig Oresjo that included over 1 billion solder joints and multiple EMS and OEM manufacturing sites.

No single test solution covers the entire fault spectrum -- a combination of methods is required to ensure full fault coverage. An integrated test approach with complementary value-added by each test station is more often the optimal strategy.



**What ATE Hardware is
Right for Your Products?**

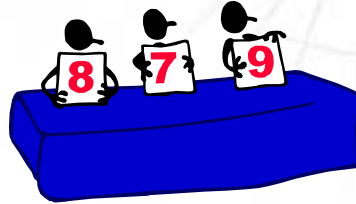
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There are Many Dimensions to the Test Strategy Evaluation Matrix

Different Test Methods Exhibit Varying

- fault coverage
- diagnostic resolution
- throughput
- cost
- confidence to ship
- time to debug
- time for test development



Determining the right test strategy is a problem with many dimensions of complexity!

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Electronics manufacturers have a multitude of issues to consider when designing test strategies for their PCBAs; a variety of tools including AOI, AXI, flying probe and in-circuit test are available.

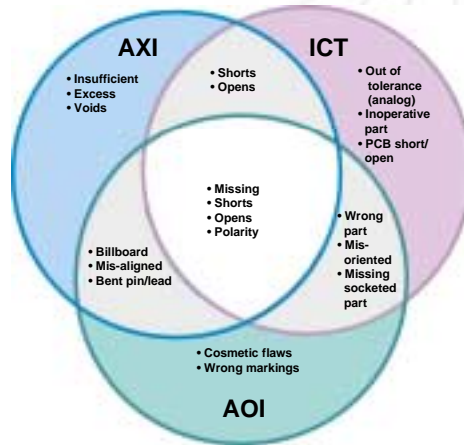
Each test method has varying performance levels along many different characteristics like fault coverage, test speed and time for test development.

Determining a test strategy from a matrix with so many dimensions of complexity, is no easy task. One can imagine the evaluation matrix growing to unmanageable proportions.

Without an effective quantitative analysis approach, the high number of choices and convoluted, overlapping characteristics can make optimizing a test strategy very difficult, time consuming and lead to questionable results at best.

Fault Coverage by Test Solution

- Each test / inspection technique has strengths and weaknesses
- Fault coverage is just one dimension of the test strategy evaluation matrix



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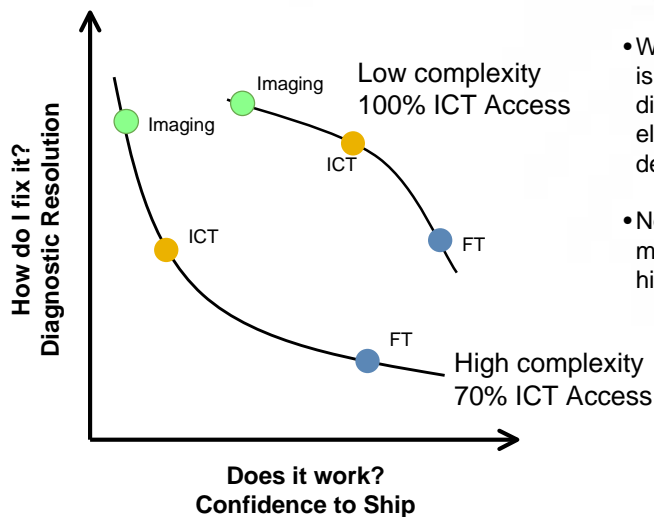
If we look at just 1 dimension of the evaluation matrix which is fault coverage we can see that each technique has strengths and weaknesses, some unique, some of which overlap with other methods of test.

AXI has strength for solder reliability, AOI for part markings and ICT for parts out of tolerance.

Note that all methods can find shorts, opens and missing parts on accessible devices.

A combination of test methods is required to cover the entire defect spectrum.

Diagnostic Resolution and Confidence to Ship



- When electrical access is reduced, the diagnostic resolution of electrical test methods decreases dramatically.
- Note that imaging methods do not provide high confidence to ship.

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Next let's look at diagnostic resolution and confidence to ship.

By “diagnostic resolution” we mean “the ability to identify the exact nature of a failure for quick and immediate corrective action...”solder open on pin 12 of device U56 for example”.

And by “confidence to ship” we mean “functional verification of the product such that we have confidence it will operate as expected in the customer environment”.

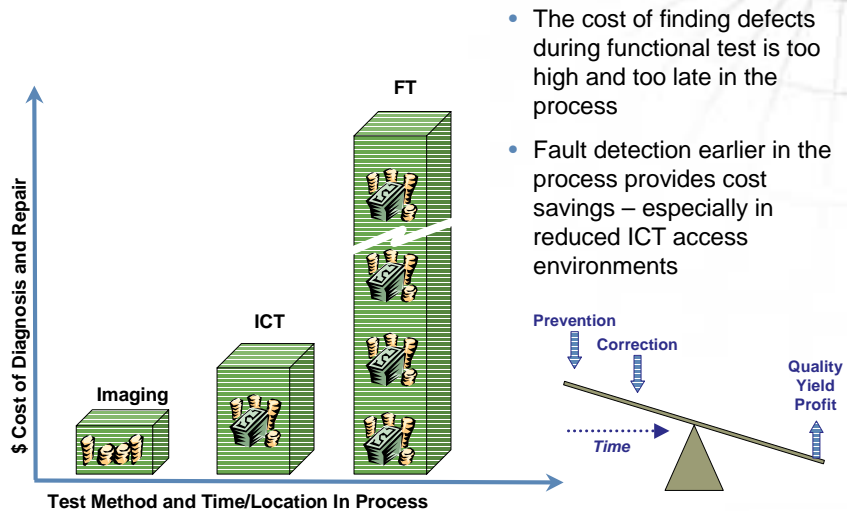
Functional test has high confidence to ship but poor diagnostic resolution.

Whereas imaging methods like AOI have high diagnostic resolution but poor confidence to ship.

Performance varies with the level of access and note that boards with reduced ICT access suffer significant declines in diagnostic resolution.

Since both diagnostic resolution and confidence to ship are important in a test strategy, a combination of test methods is required.

Cost of Diagnosis and Repair



- The cost of finding defects during functional test is too high and too late in the process
- Fault detection earlier in the process provides cost savings – especially in reduced ICT access environments

Building upon the concepts of the previous slide we know that...

The cost of finding defects during functional test is too high and too late in the process

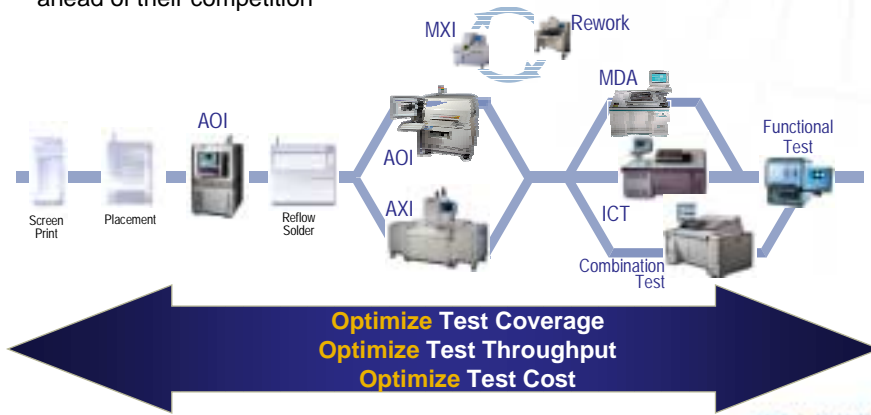
And that

Fault detection earlier in the process provides cost savings – especially in reduced ICT access environments

This again points to the use of imaging methods like AOI further up the line, closer to the source of defects to provide fault coverage and actionable information to facilitate quick debug, repair and continuous flow manufacturing.

Integrated Test Strategies that Combine Electrical & Imaging Methods Solve the Test Strategy Challenge

- Most products need both electrical test and automatic inspection to meet the quality requirements of today's customers
- Manufacturers that optimize the use of their test and inspection assets stay ahead of their competition



We've reviewed technology trends in ATE like reduced ICT access and the introduction of lead free solder that are creating a need for imaging methods like AOI and AXI to complement Manual Visual, ICT and FT methods.

We've also reviewed that no test method has coverage over the entire fault spectrum and that each method of test has strengths and weaknesses according to important criteria like diagnostic resolution and confidence to ship.

These are the technology drivers for integrated test strategies.

The bottom-line is that:

- Most products need a combination of electrical test and automatic inspection to meet the quality requirements of today's customers

But what are the strategic business reasons for pursuing integrated test solutions?

What are the benefits to the financial bottom line?

Next...Let's explore why

- Manufacturers that optimize the use of their test and inspection assets can stay ahead of their competition...

How Can Test Strategies Help You Gain Competitive Advantage?

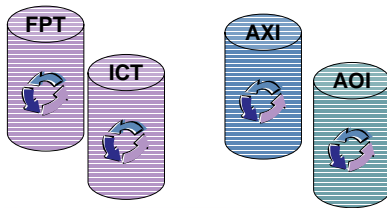
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Traditional vs. Integrated Approach to Test and Inspection

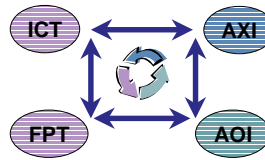
Traditional Approach

- Select test equipment without consideration of inspection equipment (& vice-versa)
- Over programming each tool
- Overlapping T&I
- Little management of overall fault coverage or test strategy



Integrated Strategy

- Provide highest overall test effectiveness at lowest cost
- Develop optimal test strategy during the design phase
 - Leverage strengths of each platform to minimize weakness in others
 - Reconcile coverage gaps before production
- Coverage management, verification and feedback



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Lets examine the attributes of a Traditional approach to Test and Inspection vs. a new Integrated Strategy that can deliver competitive advantage....

In the traditional approach...

We select test equipment without consideration of inspection equipment (&vice versa)

We often over program each tool beyond its core strengths...this means we can spend more time in test development with diminishing returns...sometimes 80% of the fault coverage can be attained in the first 20% of program development time.

We often have lots of overlapping test and inspection coverage...this can cause longer production test times higher fixture costs, and longer fixture build times.

We have little management or up-front planning of the overall test strategy.

In a traditional test and inspection approach, inspection tools are often owned by process engineers and electrical tools by test engineers with little cross-communication or information sharing. There is little understanding of the overall fault coverage and little coordination to deliver benefits like improved time to market.

In an integrated strategy however...

We aim to provide the highest overall test effectiveness at lowest cost independent of any 1 test stage.

We develop the optimal test strategy during the product design phase and leverage the strengths of each platform to minimize weakness in others

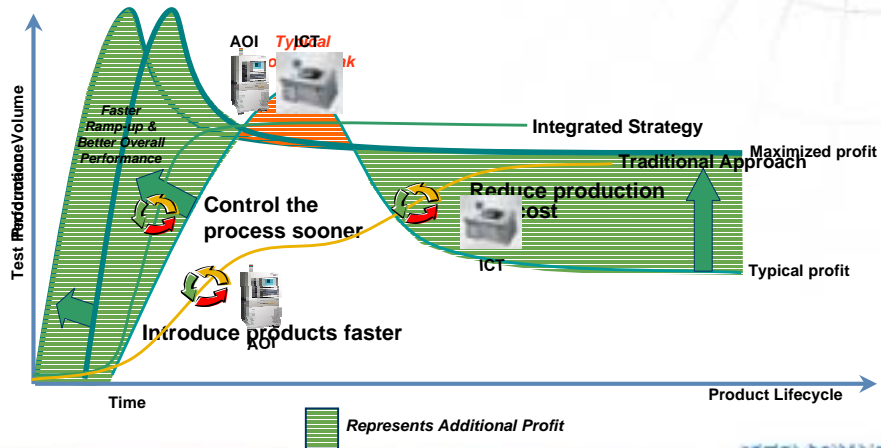
And we reconcile coverage gaps well before production because we have the ability to plan our test strategies early.

Finally, we have coverage management, verification and feedback

A managed and integrated system to ensure we plan, then implement then verify we got what we paid for in the first place.

Well-Designed Test Strategies Gain Competitive Advantages

Electronics manufacturers can achieve a competitive advantage by integrating inspection, test and related engineering activities into an integrated solution rather than optimizing single point solutions.



In today's world of electronics manufacturing there is ever increasing pressure to reduce cost, increase quality and shorten time to market. Test can be used to gain advantage in a competitive environment by driving cost reductions through the entire product lifecycle from design, through New Product Introduction, manufacturing and warranty.

In the next few slides, we'll review how Teradyne integrated test solutions help

- Introduce products faster to improve time to market
- control the process sooner for faster production ramp and
- reduce production test costs

[Animate 1]

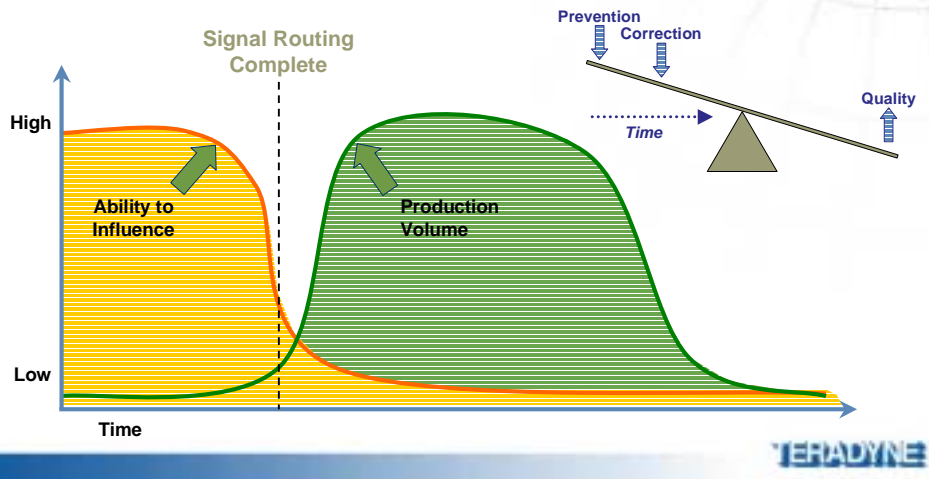
Rather than optimizing point solutions in a traditional approach to test and inspection,

[animate 2]

electronics manufacturers can achieve a competitive advantage by integrating inspection, test and related engineering activities into a single system for faster ramp and better overall performance

Plan Test Strategies Early to Maximize Benefits

Test strategies planned early in the product life cycle, provide greater fault coverage, yield and profitability for less net expense and faster time to market.



When manufacturers can plan test strategies early in the product lifecycle, they can consider various test alternatives, the cost and coverage of each and select the optimal strategy before a single board is ever manufactured.

When ICT access is constrained due to high IO densities and signal integrity requirements, test pads need to be placed where they provide the most fault coverage. Teradyne Test software “d2B Strategist” can be used prior to the layout routing stage of PCB design to determine which test pads provide the highest non-overlapping fault coverage in a distributed test environment so that designers can place test pads where they are most required.

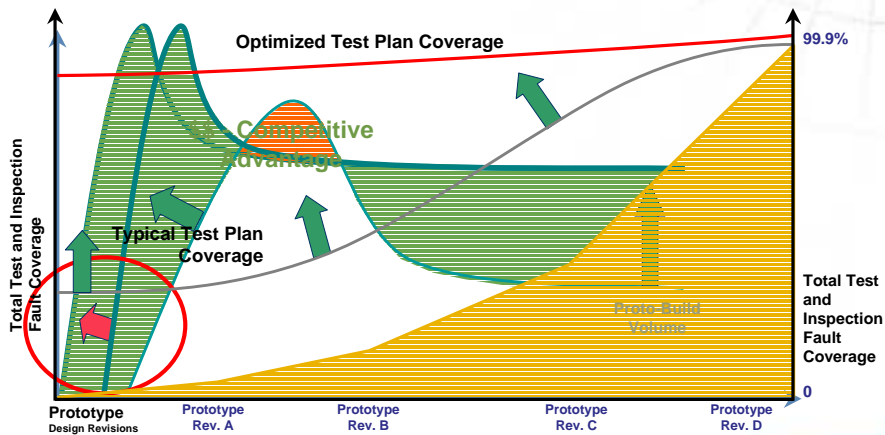
After the layout routing stage of PCB design, test engineers have little or no influence on the location of test pads.

In this way, manufacturers can manage loss of access, ensure higher fault coverage and influence manufacturing methods early in the product life cycle to ensure lowest cost of test.

Teradyne test solutions support these requirements early in the product design, prior to layout routing.

Faster NPI Improves Time to Market

Integrated test strategies planned early in the life cycle can ensure the highest fault coverage before a single board is ever manufactured.



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Lets talk more about “time to market”

Companies that satisfy consumer demand for innovative products early in their life cycle win both market-share and profits.

[animate 1]

Manufacturers typically go through several prototype iterations before ramping production. Each iteration of the prototype is used to perfect the product design, manufacturing process and test coverage.

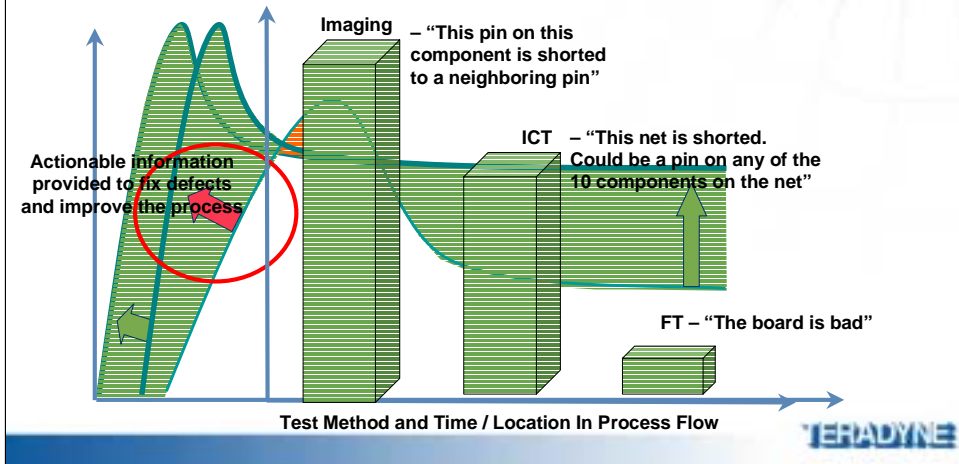
Uncovering design flaws is linked to how good the test coverage is for that prototype, which is why several iterations are required. The main reason why test coverage is not as high as it could be during the first prototype is that evaluating the board design and predicting the fault coverage of a specific test strategy is an extremely engineering intensive activity.

Teradyne’s Strategist software creates a new paradigm. Performing test point optimization and developing the most effective test strategies is done in minutes rather than days which ensures high test coverage for each prototype revision.

Depending on the type of board, having the optimal test strategy developed before starting any kind of manufacturing could cut days or even weeks out of the prototype revision phase of a product.

Control the Process Sooner

- Test and inspection integration allows:
 - Use information to improve process and minimize WIP, RIP and scrap
 - Use predictive tools to focus attention on likely problem areas



Lets talk about “controlling the process sooner”...

[animate 1]

As electronics assemblies become more complex with increased functionality and higher IO,

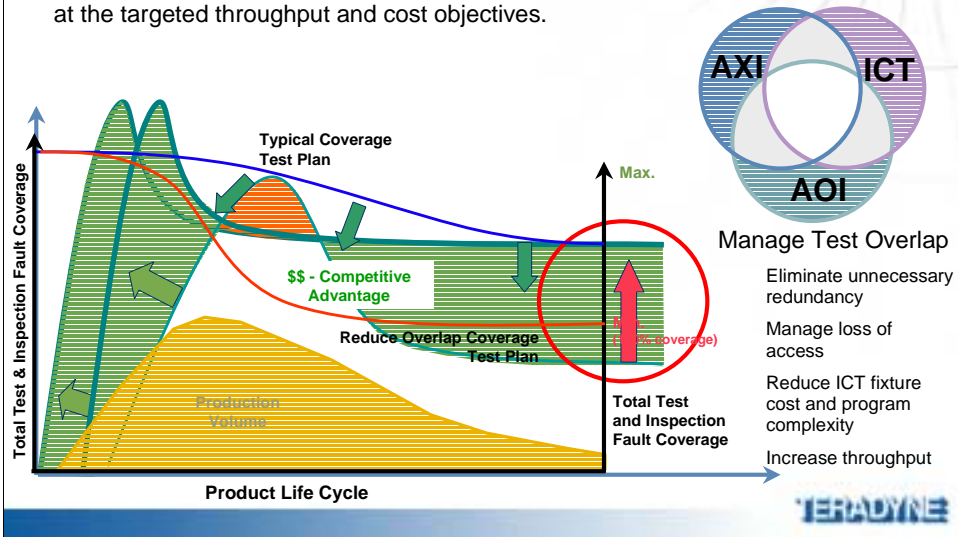
limited diagnostic resolution can sometimes ‘roadblock’ manufacturers from objectives like ‘continuous flow manufacturing’ and higher inventory turns. The time required to debug defects at ICT and FT can be prohibitive. As manufacturers face increased pressures to reduce cycle time and WIP, they are looking for test solutions that reduce time spent in debug and repair cycles.

For the 80% to 90% of the fault spectrum that consists of structural defects, Imaging methods provide the highest amount of actionable information for fast diagnosis and repair, reduced WIP and reduced scrap.

Furthermore, if manufacturers can plan test strategies and predict where faults will occur, they can focus attention on likely problem areas to facilitate process improvement and faster ramp. We’ll talk more about the predictive nature of Teradyne solutions a little later in the presentation....

Manage Test Overlap to Reduce Production Test Costs

Optimize test strategy to provide the right amount of test coverage at the targeted throughput and cost objectives.



Lets talk about reducing production test cost...

[animate 1]

In this particular example a manufacturer of a high volume non-mission critical electronic device can reduce production test costs after the ramp phase has been completed and there is sufficient confidence in the stability of the manufacturing process, by eliminating redundancy in the test plan - while still maintaining full coverage.

Teradyne Strategist solutions identify overlap and provide strategies that will reduce test redundancy and thereby reduce test costs.

Savings can usually be gained in the form of reduced capital expenditure, reduced fixture cost and improved throughput.

Unlike this example, other types of PCBAs like military or aerospace boards that are destined for high reliability applications often require overlapping test coverage to minimize the possibility of defect escapes. Understanding that no test method is perfect, some manufacturers prefer a high level of overlapping fault coverage and test redundancy to ensure all possible defect opportunities are sufficiently screened.

Teradyne Strategist software supports both these strategies and enables users to identify the degree of fault coverage overlap necessary to meet the quality and reliability requirements of the end use environment at the targeted throughput and cost objectives.

Reduce Production Test Costs: Warranty & Field Failures

Ensure coverage of the entire fault spectrum for

- Higher Shipped Quality
- Higher Customer Satisfaction



Failure costs can be high and far-reaching

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As technology plays a more critical role in our everyday lives, uptime and reliability are key concerns. Modern commerce can create immense liabilities and field failure costs for companies that do not meet the demands of the marketplace.

Field return rates, warranty costs and customer satisfaction are substantial liabilities for all electronics manufacturers.

The shipped quality level provided by a test strategy is a key performance metric and should be factored-in to calculations of production test cost.

Teradyne solution provides engineers with the ability to identify where they do and where they do not have test coverage to ensure highest fault coverage possible.

Manufacturers can evaluate whether their test plan meets the reliability requirements of the end use environment at the earliest stages of product development, within minutes - not days.



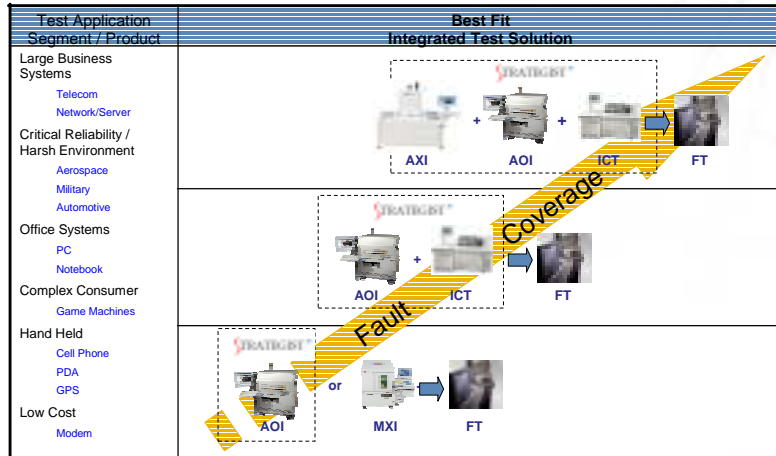
**What Tools Does Teradyne
Offer to Help You Design
Best-In-Class Test Strategies?**

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Teradyne Test Solutions

Teradyne offers an integrated suite of scalable solutions to meet any product test requirement



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Teradyne offers an integrated suite of scalable solutions to meet any product test requirement.

With the Design2Build Strategist software, we can integrate any combination of the industry's broadest offering of test and inspection solutions.

For low cost, high volume products like cell phones and PDA's we can combine Strategist with our 7200 or 7300 imaging systems to provide highest throughput and excellent fault coverage.

For products that have higher defect opportunities like office systems and high reliability automotive electronics, we can combine our industry leading installed base of In-circuit testers like Test Station, Spectrum and Z1800 with either AOI or 4010 series of automated x-ray products.

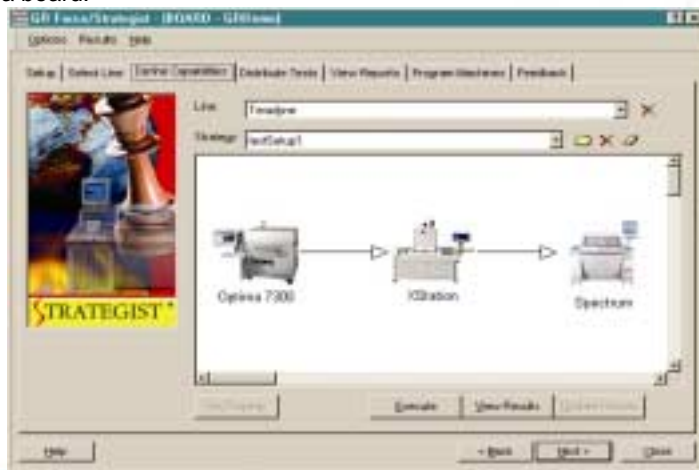
And finally for the highest defect opportunity and critical reliability products like telecom infrastructure, Strategist combined with each of our test, optical and x-ray platforms provide maximum fault coverage.

For all solutions, manufacturers also receive the benefit of identifying potential escapes to functional test so that functional test coverage and diagnostics can be optimally designed.

For any application, Teradyne offers a fault coverage solution at the targeted throughput and cost objectives demanded by different segments of the electronics industry.

Predict Test Strategy Performance Using Teradyne Solutions

Model different line configurations and compare fault coverage, yield, test times and line effectiveness from your desktop in minutes without ever building a board.

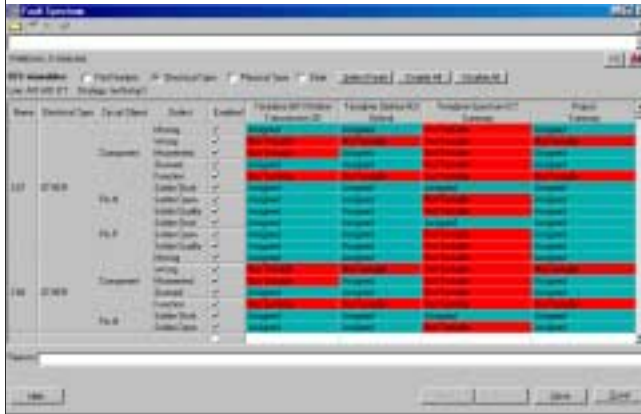


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Teradyne test strategy solutions enable electronics manufacturers to model different line configurations and compare fault coverage, yield, test times and line effectiveness from the desktop in minutes without ever building a board.

Users can modify test coverage assumptions on the equipment to suit their unique environment and even make use of ICT device libraries to accurately predict fault coverage.

Benefits of Predictive Fault Coverage and Test Times



- Ensure quality, verify the entire fault spectrum is tested
- Optimize placement of test pads for boards with limited ICT access prior to layout routing
- Influence customers & partners with test strategy data
- Improve quoting accuracy by selecting the optimal test strategy early in the product life cycle

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The benefits of predictive fault coverage and test times are:

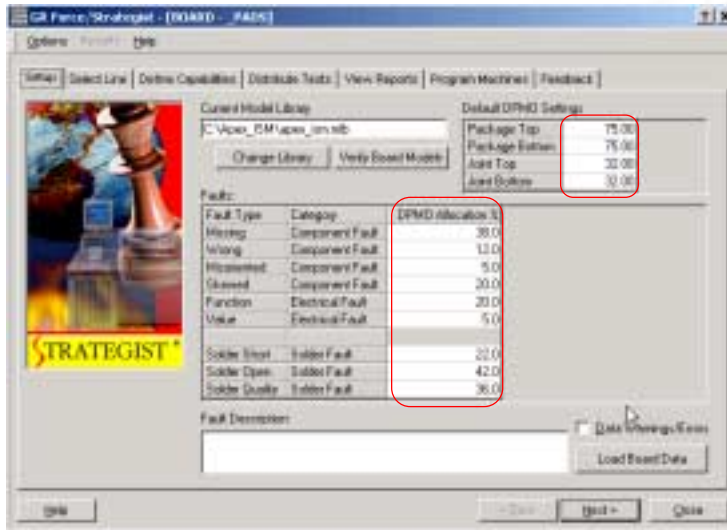
To ensure quality by verifying that the entire fault spectrum of a board is being tested. The chart shows how Strategist software models every component and pin on the board, all the defect opportunities on each component and pin – electrical and structural – and which test stages have coverage of each defect.

To optimize the placement of test pads for boards with limited ICT access prior to the layout routing stage of PCB design

To influence customers & partners with test strategy data by using quantitative reports to demonstrate that the correct fault coverage is being attained at the targeted throughput and cost objectives.

To improve the quoting accuracy of PCB test and assembly work by more accurately predicting yield, quality and cost targets using the limited amount of data that is available at time of quotation

Input DPMO Data to Accurately Measure Coverage and Yield



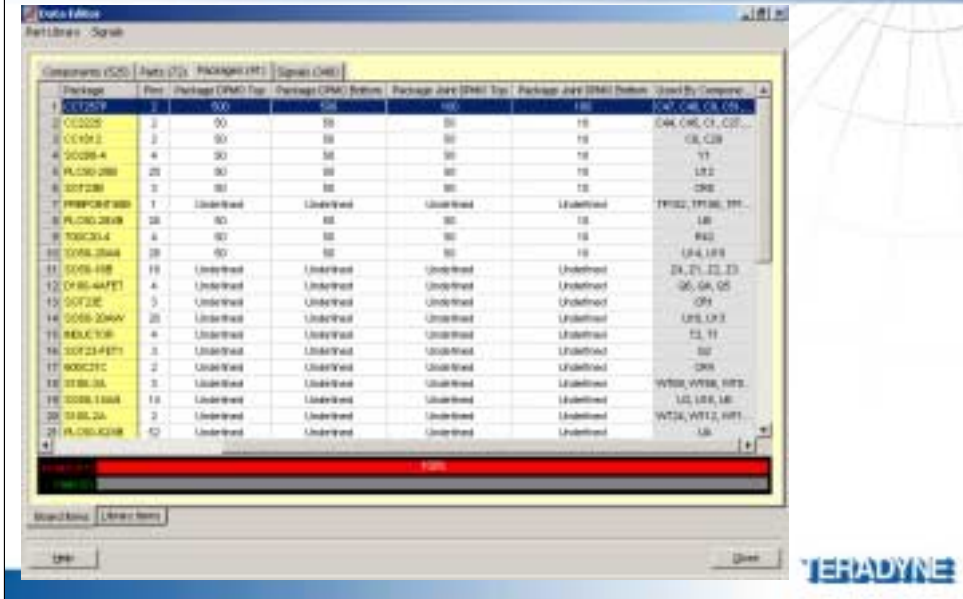
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Manufacturers can enter Defect per Million Opportunity rates reflective of their own manufacturing environment to more accurately measure test coverage, yield and shipped quality levels.

If DPMO statistics are not available, default assumptions can also be used.

In this chart, we can assign dpmo rates for packages on the top and bottom sides of the board independently. In addition, we can allocate higher DPMO rates to defects that are more common in the process, thereby giving a more accurate prediction of coverage and yield.

Create DPMO Libraries by Package Type

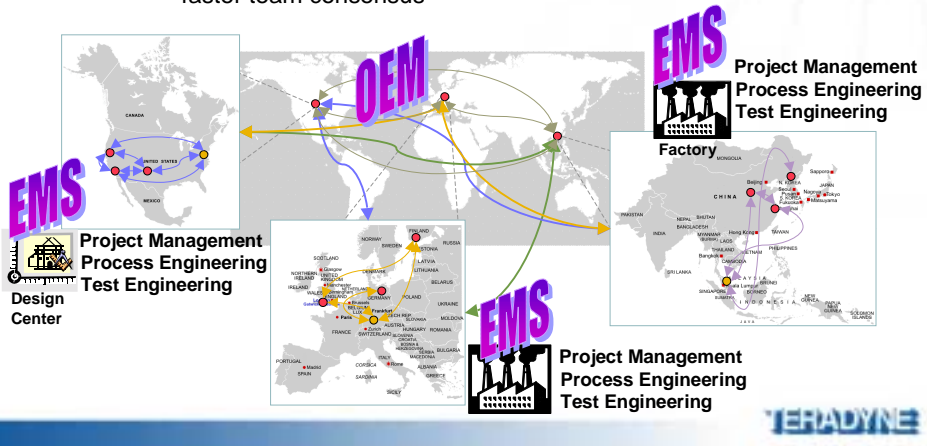


Stratigent allows users to create DPMO libraries by package type. These libraries can be used as a quality database and continually improved over time to deliver more accurate results.

Global Supply Chains Create Communication Challenges

Accurate information and effective communications are fundamental to building better partnerships in your global supply chain

→ Need a common language to discuss test strategy issues for faster team consensus

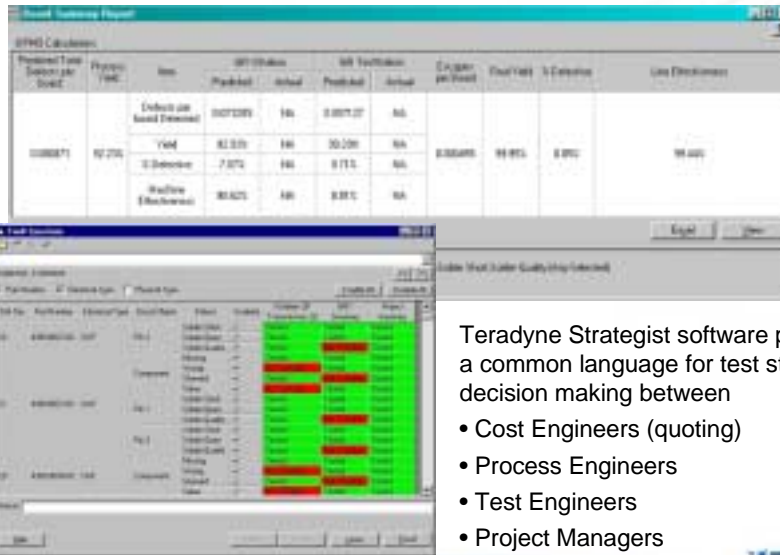


As EMS providers expand their global presence, accurate information and effective communications are fundamental to building better partnerships in their supply chain.

Test coverage, quality, DPMO and yield are some of the most inconsistently measured performance criteria in the electronics industry. Regardless of language barriers, cultural differences and geographic distances, even a common language on technical matters related to test is hard to find. For companies that want to operate as a unified global company and project a 'single-face' to multi-national customers, this poses a real challenge.

Both OEMs and EMS providers need a common language to discuss test strategy tradeoffs to achieve rapid organizational consensus and influence their partners' manufacturing strategies.

Create a Common Language for Test & Quality Decision Making



Teradyne Strategist software provides a common language for test strategy decision making between

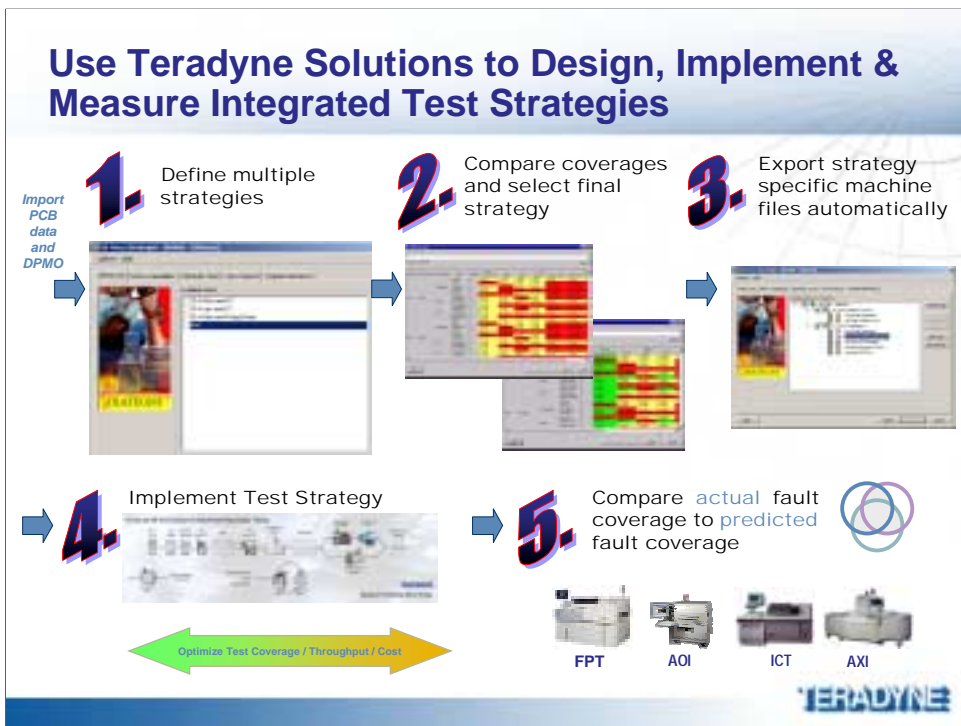
- Cost Engineers (quoting)
- Process Engineers
- Test Engineers
- Project Managers

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Teradyne Strategist software provides a common language for test strategy decision making between OEMs and EMS providers.

Strategist reports quantify fault coverage both on what *is* tested and what is *not* tested at each test stage for every pin on every device on the PCBA. In addition, summary reports identify test times, test yield, DPMO and test effectiveness - All in minutes at the earliest stages of the product development cycle.

By helping organizations quantify tradeoffs related to fault coverage, yield, and cost, Teradyne solutions help them communicate, manage expectations and build partnerships within their supply chain.



Teradyne offers manufacturers a complete test strategy management solution at each stage of the product life cycle...

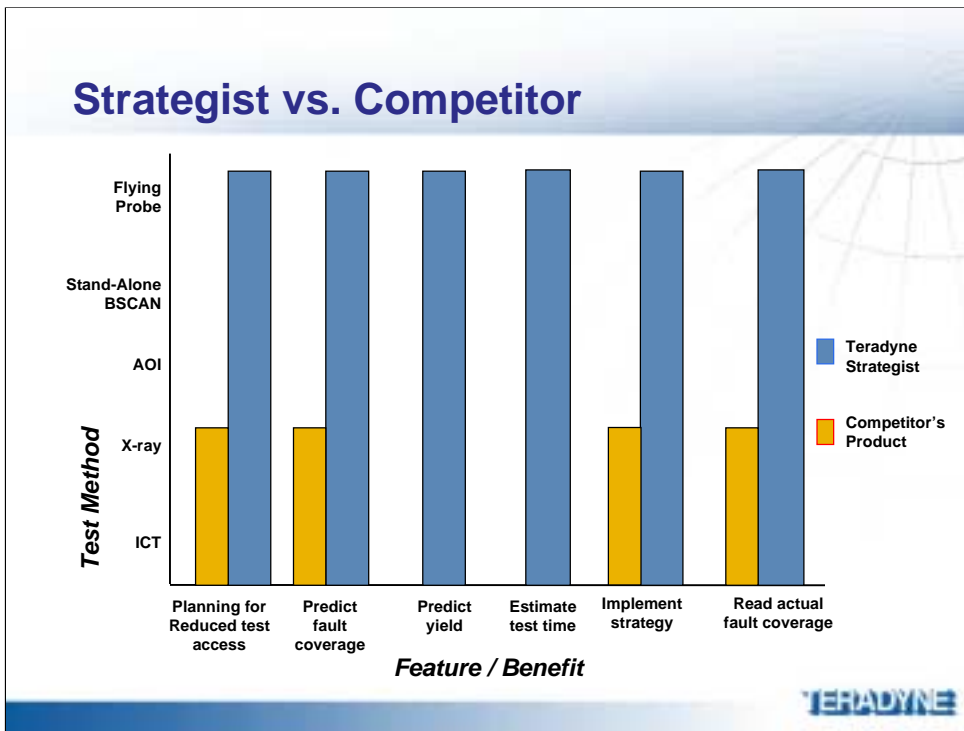
From quoting and the ability to model different strategies and select the best approach...

To design and the ability to plan for loss of access...

To implementation and the ability to export strategy specific machine files to production line test machines...

To verification and the ability to feedback actual production fault coverage and compare to what was predicted earlier in the cycle.

Teradyne offers a complete and integrated system to manage test and verify you got what you paid for in the first place.



Teradyne's full featured test strategy software is unique in the marketplace.

The chart shows Teradyne capabilities vs. those of the nearest competitor.

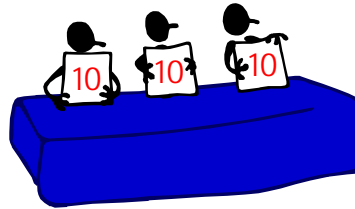
On the vertical axis, we can see Teradyne Strategist covers a broader set of test equipment choices including ICT, AOI, AXI, Stand-alone boundary scan and flying probe test.

On the horizontal axis, we can see the capability includes planning for reduced test access, performing both predictive and actual fault coverage analysis and yield estimation.

Teradyne Solutions Maximize Performance

- Teradyne provides the tools to integrate test and inspection components into a single system to help customers maximize all of the following:

- ✓ – fault coverage
- ✓ – diagnostic resolution
- ✓ – throughput
- ✓ – cost
- ✓ – confidence to ship
- ✓ – time to debug
- ✓ – time for test development



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Teradyne provides the tools to integrate test and inspection and related engineering activities, into a single managed system.

This enables manufacturers to develop best in class test strategies that deliver improved fault coverage, diagnostic resolution and throughput and cost.

Key Points: Integrated Test Solutions

- The combined use of imaging and electrical test methods helps overcome the test strategy challenge
- Integrating test and inspection into a single managed system provides a means for your manufacturing organization to gain competitive advantage
- Determine the optimum test strategy early to influence manufacturing methods and plan for loss of ICT access
- Improve quoting accuracy and build consensus through your supply chain by using quantitative methods to determine the optimal test strategy
- Measure performance of implemented strategy (predicted vs. actual) to ensure ongoing effectiveness

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Lets summarize some key points.

The combined use of inspection methods and electrical test methods helps overcome the test strategy challenge.

Integrating test and inspection and related engineering activities into a single managed system with tools like "Strategist" provides a means for your manufacturing organization to gain competitive advantage.

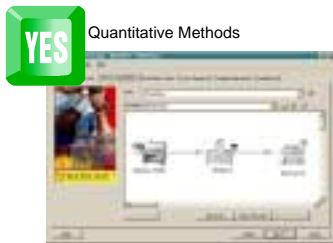
When we determine the optimum test strategy early in the product design to influence manufacturing methods and plan for loss of ICT access, we attain faster time to market and reduced production test cost.

We can improve quoting accuracy and build consensus through the supply chain by using quantitative methods to determine the optimal test strategy. We can use reports that summarize test effectiveness, yield and fault coverage to influence customers and partners on test strategy decisions.

Its important to measure the performance of the implemented strategy to verify you got what you paid for in the first place. By providing the capability to compare actual fault coverage on the production floor vs. that which was predicted during product design, software tools like Strategist help ensure ongoing effectiveness and continuous improvement of product test strategies.

Conclusions

- Teradyne test solutions help you determine the best integrated product test strategy for competitive advantage



- “Crystal ball” test strategy development is not acceptable

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In Conclusion...

Engineers have often used past experience or subjective preference as a means for assigning test strategies to new products without analyzing the benefits and weaknesses of various different test approaches in a quantitative manner.

Modern PCBAs in our cost and quality competitive environment require a more optimized strategy for each and every board manufactured.

Teradyne test solutions can help you determine the best integrated product test strategy for competitive advantage

Thank you!

- A recording of this event will be posted at <http://teradyne-events.webex.com>
- For More Information on Teradyne Products, Call Us at 1-800-TERADYNE, or Go To <http://www.teradyne.com/cbti>

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This concludes Teradyne's presentation of "Designing Test Strategies for Modern PCB assembly".

Thank you for attending.

In the near future, you will receive an email with a link to the recorded version of this web seminar as well as posted questions and answers.

Should you desire any further information on our family of Assembly Test Products, call us at 1-800-TERADYNE or go to our web site, which is www.teradyne.com/cbti

Enjoy the rest of your day.