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Testing Multi-Functional Power Management ICs

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Cell phone functionality and battery life drive the PMIC market. New test strategies enable faster silicon debug and a quick release to production.

The evolution of the cell phone is marked both by growth in units shipped and a constantly increasing feature set. Manufacturers add these features under the competitive pressures of minimizing cost and maximizing talk time. Power management ICs (PMICs) perform critical functions in realizing advanced cell phone and smart phone capabilities. The PMIC's core function is to efficiently distribute battery power to as many as 25 different applications within the phone, many of which require unique voltage and current. Additionally, in an attempt to cover the growing feature set, PMICs perform a variety of other system functions. These blocks may include audio codecs and amplifiers, general-purpose analog/digital and digital/analog converters, touch-screen interfaces, light-emitting diode (LED) and vibration motor drivers, USB2.0 interfaces and real-time clock (RTC) buffering circuits. Figure 1 illustrates a generic, highly integrated PMIC.

PMICs currently contain 80-300 pins and are trending upwards. The PMIC business is highly competitive. A missed technical target or delivery date can mean the complete loss of a design-in, which translates to a substantial business loss. All of these complexities provide a set of challenges and pressures for the test engineering organization whose critical tasks take place immediately prior to sample delivery and product shipment. The challenge can be summarized as increasingly complex IC test solutions that must be developed and qualified more quickly and for reduced cost.

Several essential automatic test equipment (ATE) capabilities are required by PMIC manufacturers in order to meet the demands of their market. These capabilities fall into two categories: system level and instrumentation. At the system level, the tester must provide a software environment that enables rapid debug of new silicon and quick release to production.

The ATE must also support efficient multi-site testing. Well-aligned instrumentation forms the basis of a solid configuration.

PMIC test capability

A standard PMIC tester will contain power supplies, programmable voltage/current sources (VIs), AC waveform source and capture, and high-speed digital instrumentation. VIs are critical instruments for addressing the test requirements of these devices. The defining characteristic of a VI is its ability to force and measure current or voltage in four quadrants. VIs need to go beyond meeting the base voltage and current characteristics of the device under test. The VI needs to be capable of:

- Accurate differential measurements with relatively high common mode voltages.
- Repeatable measurements with optimum throughput.
- Efficient voltage threshold search.

These critical characteristics map to the tests for a common sub-block of the PMIC, the switched-mode power supply (SMPS). Today SMPSs are primarily single-phase, inductive buck regulators with integrated power field-effect transistors (FETs) (Fig. 2). Although boost converters (both switched capacitor and inductive) also appear, the buck regulator is most common. The performance criteria of an SMPS include efficiency, transient response, ripple, and line and load regulation. All of these criteria directly or indirectly affect battery life.

Test lists typically emphasize parametric over functional tests because of the difficulty of realizing ideal performance through a test socket. Tests such as RDS_{on}, current limit or short circuit current, and leakage focus on the power FET component of the block. Timing measurements are made by the pulse-width modulator (PWM) controller. Numerous threshold measurements are applied to the block to verify startup/shutdown due to over- and under-voltage conditions, over-current, as well as other thresholds that depend on the SMPS topology.

Source/drain resistance

We first discuss RDS_{on}, which is a measure of the resistance of the FET, between the drain and source pins, while the FET is "on." The typical value of this resistance is in the milliohm range, but often requires measurement at high voltage and current levels, depending on the operating conditions. These FETs are also often configured in circuits where they are "floating" or not directly connected to ground. What is needed is an instrument that can measure a very small differential voltage across the FET drain-source, in conditions where a high voltage and current referenced to ground is present.

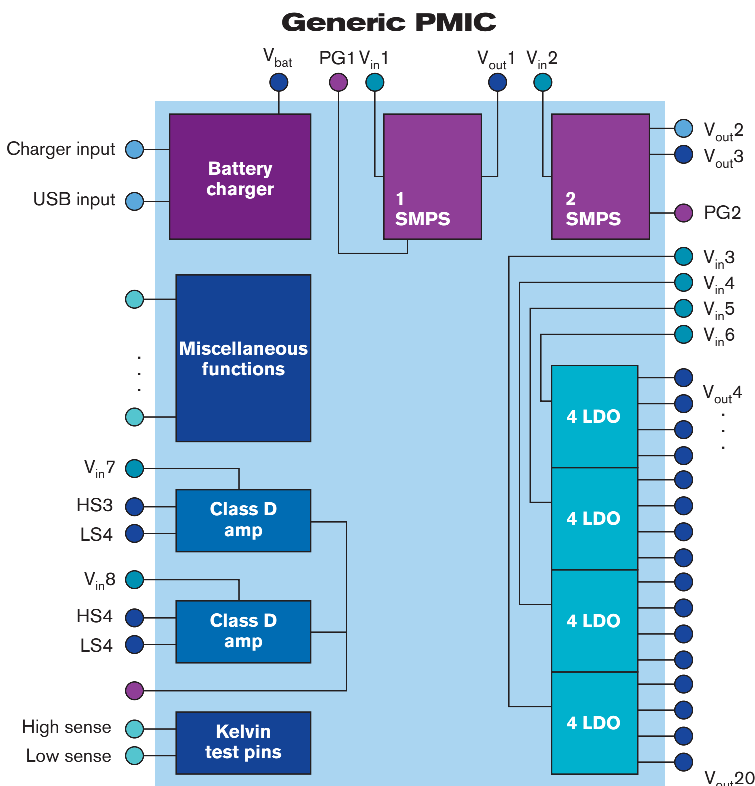
An integrated, high-density differential voltage meter allows accurate, small measurement to be made at a relatively high common mode voltage. For example, an RDS_{on} measurement of a power FET could be made in a 50 mV meter range at an offset of 3 V. RDS_{on} is a critical predictive measurement for both efficiency (Fig. 3) and transient response of the SMPS.

The RDS_{on} test also requires comprehensive, easy-to-use software tools to optimize for test time. Imagine a device that has five SMPSs, and each SMPS block has two power FETs to be tested. A single-measurement multiplexer (MUX) is used to access each of the measurement points. The task of the test engineer should be to adjust measurement wait time in order to achieve repeatable results. The actual wait time will depend on the tester VI's dynamic behavior and the device's response to it. Achieving an optimal wait time and test throughput is greatly enhanced by having visualization tools available. The software visualization tools should allow measurement samples to be graphically displayed and provide interactive control to fine tune the wait time.

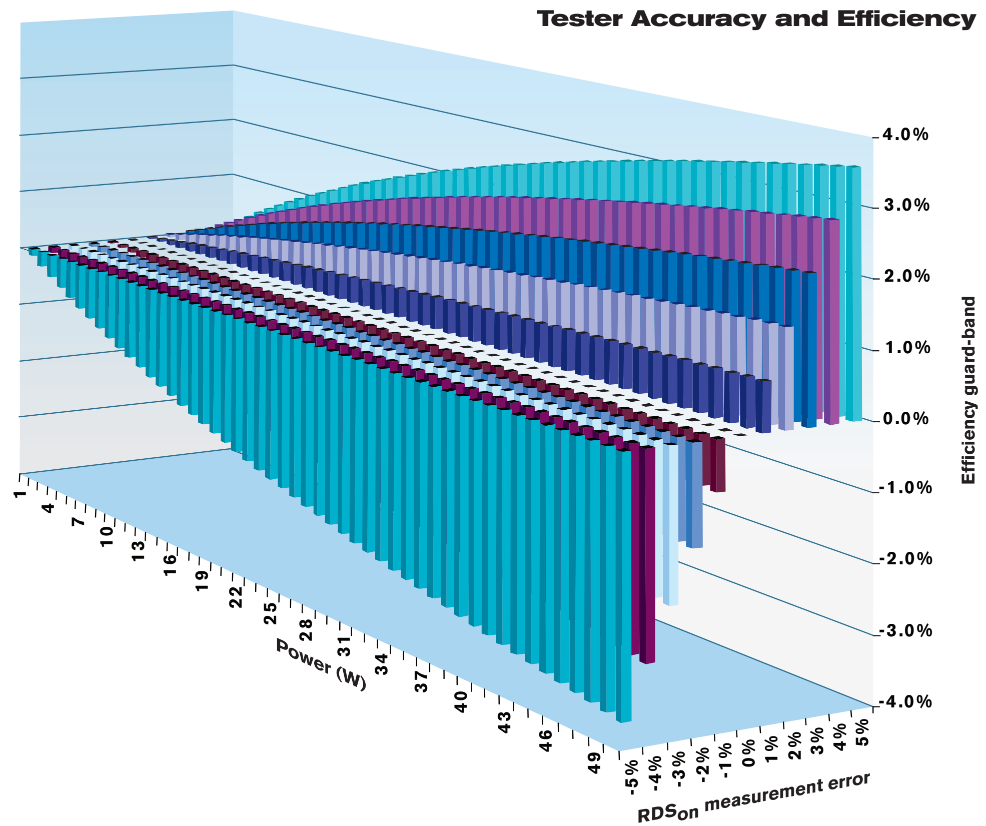
An additional feature that a test system should have is the ability to connect important device and tester system signals to a scope. For DC measurements, the critical signals are the input to the measurement meter's ADC in the VI instrument and access to the meter strobe. With these signals available on a scope, the test engineer can choose an optimized measurement point with software adjustments. For complex PMICs there are thousands of tests that require these careful adjustments to be made. Without these tester capabilities, test engineers will tend to be cautious and have longer wait times, increasing the overall test time for the device.

Comparator threshold test

The second most frequent type of tests in a PMIC is a comparator threshold test. Threshold detection is used for a variety of purposes in a PMIC, including charger voltage and current detection as well as the determination of various over-voltage, under-voltage and over-current conditions. Two methods are commonly used to determine the threshold of a comparator block. A third method is also available that provides advantages over the other two.



1. This generic PMIC layout shows the various functions and capability.



3. The correlation between tester accuracy and achievable efficiency of the end application.

The first, used traditionally as a characterization test, involves the application of a current or voltage ramp to the device "detect" pin. The output of the comparator can be measured directly by monitoring an analog output pin or indirectly by monitoring a digital register. With an analog output pin detect method, the output signal may be digitized as a ramp is slewed on the input pin across the expected range of the threshold. The time required to ramp and capture data after the threshold has been met does not increase test coverage and wastes test time.

A modification of this approach is to use a binary search of the input vs. the output result. This can be a fast and accurate approach if the device can be reset to its starting state quickly, and the window of area around which the threshold occurs is small enough to not require too much data collection.

A second option manufacturers sometimes take is a go-no approach to the threshold test. This is a fast method, but its disadvantage is that the threshold is left undetermined. The test engineer knows only that the threshold occurred to within a predefined window. The actual threshold value is not captured or recorded. Often manufactures do not choose this option because they wish to collect and analyze the actual results across lots.

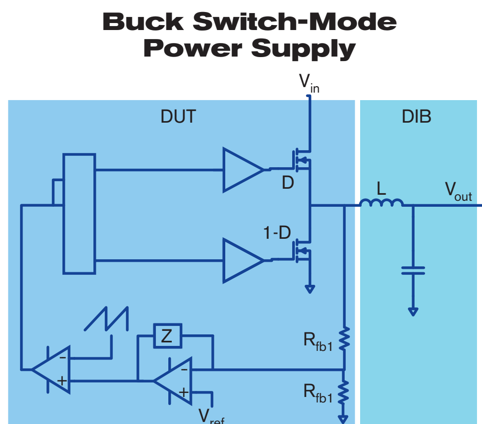
The final approach offers the advantages of the ramp search and the speed of the go-no method. In this method, the input is set up exactly the same as noted in the first example, and the output pin is monitored by a comparator within the tester (Fig. 4). When the threshold is passed, a signal is sent through the tester back to the detect pin meter, which strobes a measurement and stops the ramp at the input. This method determines the exact value of threshold level without requiring the user to digitize a large amount of data and calculate the result.

Design and test integration

Time to market for PMIC devices is very important to success of the product. Therefore, it is essential that the tester enable fast test program development and rapid device characterization. Design organizations have built libraries of design intellectual property (IP) that the PMIC designer may pull from to quickly configure the device to the customer's requirement. Time to go from final product definition to having silicon in the test engineer's hands is now measured in weeks vs. months.

ATE software must provide the tools necessary for the test engineer to quickly focus on the device functionality and performance. The essential requirement of the software environment is to enable the user to focus on the device under test.

There are a number of enablers to reach this point. The first is that the software environment must support a mechanism for code reuse. Since PMICs



2. The key performance criteria for a buck SMPS, efficiency, transient response, ripple, and line and load regulation, all affect battery life.

are created from existing IP, code reuse allows test engineers to associate test functions with design IP.

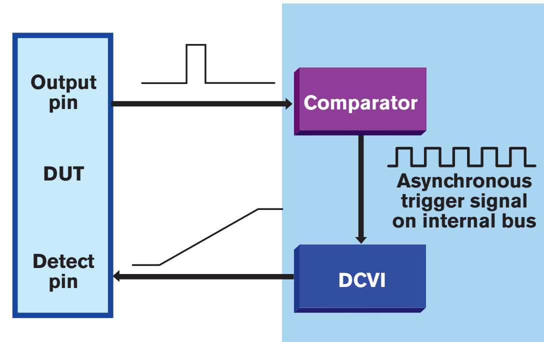
In an ideal world, design and test IP would be seamlessly integrated into the new device and work without a hitch. In reality, subtle differences occur and it is important that the tester provide a robust debug environment tailored to mixed-signal devices. Synchronized graphical debug tools for all instruments are a key component of this environment. A solid software platform allows the test engineer to immediately focus on the device when first silicon arrives. Interactive graphical debug tools provide an essential means to determine silicon performance and modify existing test functions.

In addition to these specific system-level requirements, the parallel test efficiency (PTE) of the system is a critical parameter and should be ~95% or better:

$$PTE = 1 - (T_N - T_1)/((N-1)*T_1)$$

where, T_NN is the site test time, T_1 is the single-site test time, and N is the number of sites. PMICs today are tested primarily at quad or octal site, and the differences between even a percentage change in PTE can translate to a significant throughput difference (Fig. 5).

Asynchronous Trigger Concept



4. The comparator monitors the output pin, and when the threshold is passed, a signal is sent through the tester back to the detect pin meter, which strobes a measurement and stops the ramp at the input.

Conclusion

Cell phone and smart phone manufacturers demand increasingly complex power management ICs while also driving lower cost. The ATE must enable the IC manufacturer to satisfy these needs. At the system level, a software environment must allow rapid debug and release to production. An architecture that supports high parallel efficiency allows manufacturers to take advantage of quad or octal site test. VI requirements must enable solid repeatability and reproducibility, support fast threshold determination, and be able to make accurate differential measurements. With these tester tools, test engineering organizations are well-positioned to deliver on-time, cost-effective solutions into production. **SI**

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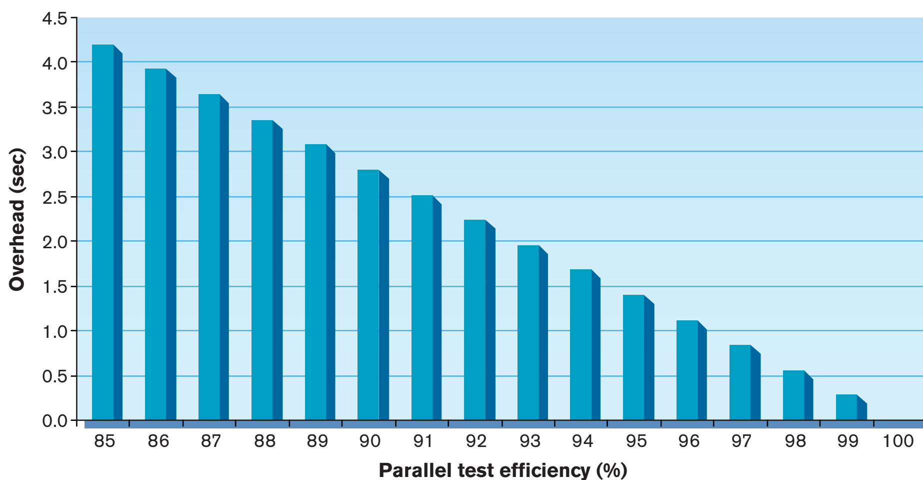
Test Efficiency



5. Shown is an octal to single-site overhead for a 4-second single-site program. Parallel test efficiency should be 95% or better to improve throughput.

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