Test & MEASUREMENT WORLD®

ZERO RE-ARM TIME MEASUREMENTS

Tests of interfaces like HDMI demonstrate the importance of measuring the timing of every clock edge.

BY TIMOTHY LYONS AND ED SENG, TERADYNE

Clock-embedded interfaces such as HDMI, Serial-ATA, MIPI, and Superspeed USB vastly increase the performance of consumer devices such as computer laptops, digital cameras, and cellphones. These interfaces improve speed and throughput by using high-quality clocks and timing references.

In the endless drive to reduce the size, cost, and power of handheld devices, multistandard semiconductor components are now designed to bridge many different interfaces. Since these interfaces use different timing standards, designers have to use sophisticated PLL, DLL, and mixed PLL/DLL clock architectures in their devices. The key parameters of these architectures include jitter, timing instability, duty-cycle distortion, and clock distortion—parameters that manufacturers must test during both characterization and volume production of a semiconductor device.

HDMI

HDMI (High-Definition Multimedia Interface) is a typical example of the new breed of high-performance, high-volume, yet low-cost interface standard. HDMI illustrates the many timing and jitter challenges that are common to the new technologies. Intended for use in consumer televisions, DVD players, and computer flat-panel displays, HDMI devices transmit full, uncompressed, high-definition video at resolutions up to UXGA and Full HD 1080p. Signals can be transmitted over 20 m to a high-definition television or a flat-

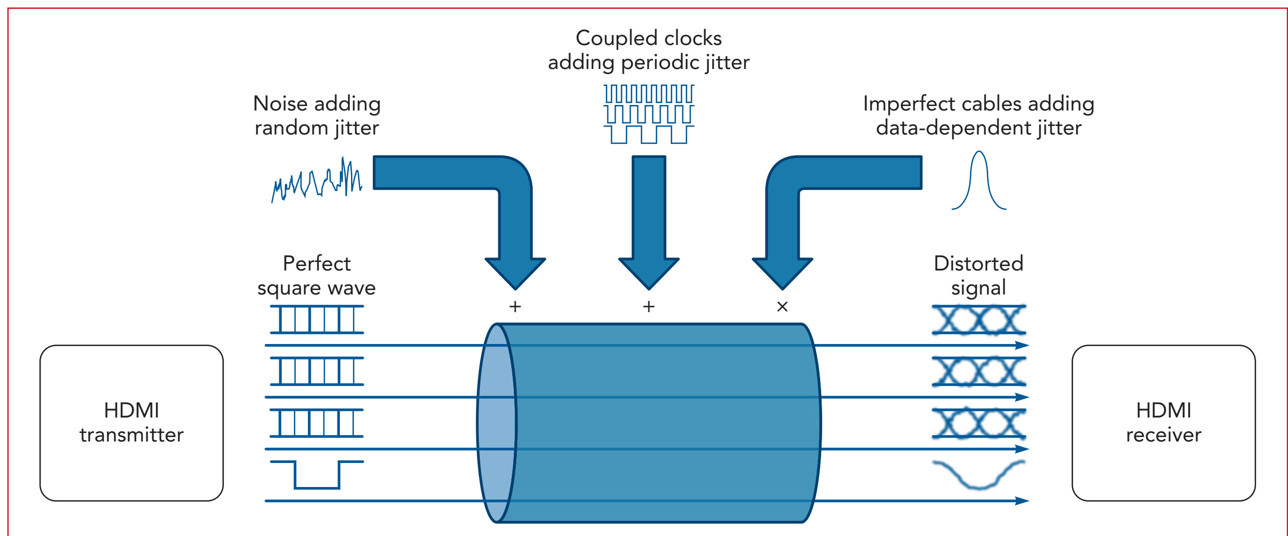

FIGURE 1. Most high-speed interfaces treat the various interfering signals as sources of jitter: random, periodic, and data-dependent.

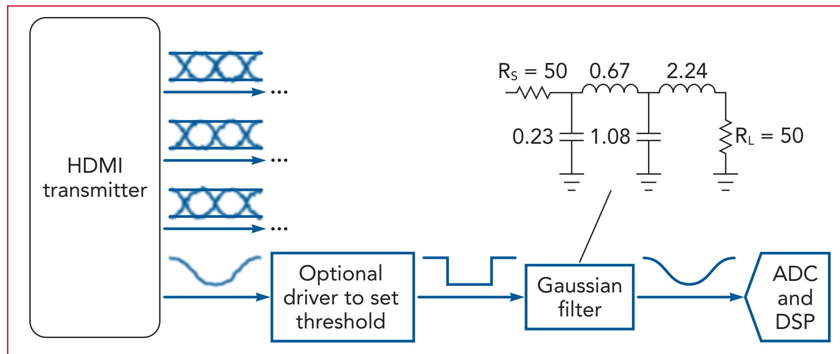

FIGURE 2. If you condition a jitter clock or a data signal by reducing its rise time to improve noise immunity and by using filtering to reduce bandwidth, an ADC in a digitizer can fully record the time position of every edge with zero re-arm time.

panel display through inexpensive consumer cabling.

HDMI 1.3 divides the video pixels into three separate data signals operating at up to 2250 Mbps. A separate 225-MHz pixel clock provides a shared coherent time base for defining the timing that the receiver circuitry needs in order to decode each of the signals it sees with an average error rate of less than one error in every 1 billion bits. In the end application, the received signal will be seriously degraded by added noise from nearby signals in a crowded printed-circuit board, resulting in what is referred to as random jitter, or Rj. When the received signal is distorted by unavoidable reflections in the imperfect 15-m consumer-grade cable or reduced in edge rise time and signal amplitude by the connectors, the jitter is referred to as data-dependent jitter, or DDj. If the received signal is time distorted by coupled clocks from nearby data signals, the result is periodic jitter, or Pj. Of course, a transmitter will also have its own noise, imperfect amplitude, slow edges, and added distortion signals.

Typical of newer interfaces (**Figure 1**), HDMI treats any distortion or noise as a source of possible timing errors at the receiver, and it budgets a maximum allowable timing instability, or jitter, for each component in the signal chain. For HDMI 1.3, the transmitter data-signal jitter is specified indirectly through an eye diagram and the differential clock reference is budgeted to a 0.3-Tbit (transmitter bit period) peak-to-peak jitter at rates above 165 MHz. The jitter and eye-diagram limits are determined relative to an ideal recovered clock that tracks low-frequency wander and jitter up to about 4 MHz. Above 4 MHz, the jitter needs to be accounted for at test.

The test of HDMI devices requires that the timing of each edge of the clock be analyzed for position and jitter content, either in early design characterization or in volume manufacturing, or both. Sometimes, early sampling will uncover timing failures inherent to a design that must be evaluated by additional testing. Over the life of a product, customers can demand that these tests continue in production test even after the underlying design weakness has been addressed.

Traditionally, clock-characterization instruments use two or three parallel time-stretching circuits to time-stamp events (an example of such an event would be a voltage crossing through a comparator threshold). The instrument might mark and record the time for a rising edge, the next falling edge, and the successive rising edge with great precision and subpicosecond accuracy for time events separated by tens of picoseconds.

But time-stretching circuits are analog in design, so after they make a measurement, they need a lengthy re-arm time, perhaps tens or hundreds of nanoseconds. In addition to the statistical issues introduced by hundreds or thousands of edges passing unmeasured during the re-arm time, the time-stamping method can be inherently slow, particularly if performed with an expensive shared, central time-measurement system or a distributed time-measurement system that must share a common data bus. Certain kinds of failures, for example an occasional PLL hiccup causing a single period that has a bad duty cycle, are particularly slow and potentially difficult to uncover. These rare duty-cycle jitter errors dictate that a device be measured many extra times to guarantee a statistical likelihood that a rare bad period will show up in a limited number of measurements. Slow tests are expensive tests.

Eliminating re-arm time

One method for improving the time-stamping test uses analog-to-digital conversion to capture every edge and perform time measurement with zero re-arm time. Low-cost, off-the-shelf USB-based digitizers can capture over 1 Gsample/s of data to characterize semiconductor device clocks operating beyond 100 MHz. Even faster digitizers capable of 4 Gsamples/s and beyond are available in PCI Express, PXI, and USB formats at a somewhat higher cost. These digitizers offer deep memory and can be easily connected to Windows-based or Linux-based computers through DLL libraries. (Rack-mount real-time oscilloscopes offer even higher bandwidths and sample rates but can be difficult to integrate into high-speed, multisite automatic test systems.)

A test system that eliminates re-arm time will let you avoid any statistical or rare error issues, because it will capture each and every cycle of a clock and derive the edge positions for every edge. In addition to providing better test coverage, recording every edge position offers excellent insight for engineering characterization and minimizes data-acquisition time by removing the need for test averaging. If the difference between a wholesome and a failing clock circuit is a hiccup once every 1000 cycles, then the acquisition will be exactly 1000 cycles long and no longer.

There are two critical issues you must manage before your test system can make accurate measurements with zero re-arm time. First, digitizers have limited analog bandwidth. Ignoring the high bandwidth of a fast-rising edge will cause the input to a digitizer to ring, clip, and distort the apparent time position of the edge and cause testing errors.

To overcome this issue, the bandwidth of the clock or data signal needs

to be reduced to match the analog bandwidth of the digitizer. You can reduce the bandwidth through careful analog filtering (**Figure 2**). A good choice for a filter is a simple approximation of a Gaussian shape by a fourth-order Bessel-Thomson (BT4) filter. Mathematically, a Gaussian filter reduces the 3-dB bandwidth of an edge to approximately 0.35 divided by the 10% to 90% rise time.

In a 50-Ω environment, you can construct a BT4 filter from four passive components. Careful selection of the filter components can reduce the time required for a sample 35-MHz clock to settle to within one-half a bit period and can reduce the bandwidth to a manageable 50 MHz or less. As long as the filter fully settles in less than one-half a bit period, there will be no time distortion of the edges. It's a good practice to use a simple model in a program like National Instruments Multisim to verify that your choice of filter components matches your expected bandwidth and rise time.

The second critical issue arises because digitizers have limited precision in the samples they record; the precision is set by the number of bits in the stored numbers. This quantization noise will introduce errors into the apparent position of the digitized edges.

To improve this limited precision, you can design your test system to perform an effective averaging by including more edges in the calculation of the position where the edge crossed the threshold or midpoint voltage. Rather than merely detecting the time when the first sample crossed the voltage threshold, signal-processing routines can use the information in samples surrounding a threshold crossing to precisely locate edges and reduce inaccuracies.

In most cases, a simple program to linearly interpolate about the zero crossing will improve the ability of the test system to locate the edge far beyond the resolution of the digitizer samples. If the test system solves a simple linear equation ($y = mx + b$) for the two samples before and after the threshold voltage, the contributing quantization error will be reduced by about 40%; more samples will reduce it further at very little additional calculation cost.

Because the BT4 filter has a fixed rise time, typically all the digitizer samples in the 20% to 80% rise time can be included in the calculation. A fit to a Gaussian curve will further refine the accuracy of the edge position as it will include even more samples in the edge location, although this further refinement will require more-sophisticated calculations and, hence, more processing time. As an added bonus, the linear and Gaussian fit routines will also reduce the errors introduced by the analog noise of the digitizer.

Using this test method, we designed a test to detect occasional duty-cycle errors in an approximately 200-MHz clock. For this device design, a failing device would exhibit a hiccup in the clock-duty cycle. The bad duty cycle was not known to be consistently distributed in the clock output, but we knew it would occur every few hundred cycles for a failing device.

The allowed maximum settling time that will minimize bandwidth without timing distortion for the 200-MHz clock is 2.5 ns, which is one-quarter the clock period or one-half the bit period. A good filter choice is a BT4 with a 1-ns 10% to 90% rise time and a consequent 285-MHz, 3-dB bandwidth. For the digitizer, we chose a 2-GHz bandwidth, quad-channel, 2-Gsamples/s, 10-bit digitizer.

The high sample rate provided three to five samples within the expected rise time. With 256 Msamples of memory, the setup could capture more than 125 ms of data, including more than 20 million edges in sequence; this was far more than necessary for detecting clock periods with a bad duty cycle, but the large number of edges gave us deep insight into the patterns of the failures. For production test, only a few hundred edges were necessary.

By managing bandwidth and providing precise digital-signal processing, you can ensure that every edge in a long succession of clock edges is accurately time-stamped and located. With this information, a test system can efficiently detect and measure period jitter, cycle-to-cycle jitter, duty-cycle errors and all other timing faults. Although we used a 200-MHz HDMI clock as an example, the test method is applicable to a broad range of digital interfaces. The technique can be quickly implemented with a digitizer, a simple filter, and a computer to process the results. T&MW

Tim Lyons *is an applications engineer in the Semiconductor Test Division of Teradyne in North Reading, MA, with 24 years of experience. He is focused on SerDes, jitter, and high-frequency analog test solutions. Lyons has an MSEE degree concentrating in digital-signal processing from Tufts University.*

Ed Seng *is an applications engineer in the Semiconductor Test Division of Teradyne, with nine years of experience in the ATE industry focused on high-speed digital, serial, and mixed-signal applications. He has a BSEE from Pennsylvania State University. edward.seng@teradyne.com.*

Reprinted with permission from PACKAGING DIGEST, Dec. 2010 / Jan. 2011. On the web at www.tmworld.com.
© A UBM Canon Publication. All rights reserved. Foster Printing Service: 866-879-9144, www.marketingreprints.com.

www.teradyne.com
978.370.2700