Where Did My Signal Go?
A Discussion of Signal Loss Between the ATE and UUT

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Abstract—Automatic Test Equipment (ATE) is now testing Units Under Test (UUTs) with signals that operate with data rates of several gigabits per second. Therefore, the test engineer must understand and account for the signal degradation through the transmission path. These high-speed digital signals typically pass through a variety of transmission media between the input/output (I/O) buffers on the ATE to the I/O buffers on the UUT. This paper highlights several considerations for the test engineer who is creating the test and system setup for a multi-gigabit per second bus. The paper discusses the contributors to DC and AC signal loss as well as methods to help minimize these losses. The paper focuses on multi-gigabit applications with matched double terminated transmission lines, but also touches on slightly slower busses with other termination schemes.

Keywords—ATE; UUT; transmission; loss; termination

I. INTRODUCTION

The path from the ATE to the UUT is a giant filter. If it is AC coupled, it is a band pass filter, and if it is DC coupled it is a low pass filter. Therefore the test engineers must carefully determine the interconnect network between the ATE and the UUT to ensure maximum signal fidelity at the destination. The primary and most obvious path to consider is the cable connecting the ATE and UUT. Although the interconnect cable may contribute a significant percentage of the signal loss, there is signal loss in all of the following elements:

- The printed circuit board (PCB) of the ATE
- The PCB of the UUT
- The connector between the ATE and the cable
- The connector between the UUT and the cable
- Any other connections such as an interface test adapter

As each digital signal flows from one transmission media to another, it experiences discontinuities in the characteristic impedance of the path, which further affect the signal’s performance. Each of these elements has measurable insertion loss coefficients. This paper describes techniques to identify the key elements in the transmission path and how to use the insertion loss coefficients of these elements to determine the approximate signal behavior at the signal destination.

The paper also discusses methods for the test engineer to:

- Combine the scattering parameter (s-parameter) coefficients of each of the elements to create an overall picture of the interconnect loss
- Estimate time domain behavior from the s-parameter coefficients

After the discussion on the losses in the signal path, the paper discusses techniques on how to reduce them. A test engineer’s use of these techniques when designing the test setup may provide both better performance and more accurate expectations.

The simulations in this paper were performed using MATLAB. The simulations use simplified transmission line models. Many of the transmission line simulations use functions from the RF-Toolbox.

II. WHERE DID THE SIGNAL GO

A. What to Look for in a Cable

There are three major parameters to consider when choosing a cable, or any other series element in the path between the ATE and the UUT. These parameters are the DC resistance of the element, the characteristic impedance of the element, and the insertion loss of the element. The following sections discuss the relative importance of each of these parameters. The discussion also includes methods to interpret the relative importance of each of these parameters.

B. A Transmission Line is also a Resistor

When designing and evaluating a transmission medium, test engineers primarily consider the characteristic impedance of the line which is \( Z_0 = \sqrt{L/C} \) along with the AC loss characteristics. Although \( Z_0 \) is important to maintain good signal fidelity at higher frequencies, the resistance of the line \( R_{Z_0} \), which is not included in the characteristic impedance, is also important to consider when determining loss in the transmission path. Analyzing the network in Figure 1 where \( R_S \) is the source resistance and \( R_L \) is the load resistance, the DC amplitude can be determined by equation 1.

\[
V_{Out} = \frac{R_L}{R_S + R_{Z_0} + R_L} V_{In}
\]  

(1)
For example consider a transmission line with $Z_0 = 50\Omega$ with an input voltage $V_{in} = 1V$. Also assume that the source resistance $R_s$ and load resistance $R_L$ are both $50\Omega$. If the total path resistance $R_{Z_0}$ including the trace resistance plus the cable resistance is $3\Omega$, and the transmission line is terminated both at the source and the load, the signal amplitude $V_{out}$ will only be $0.485V$. If the test engineer does not consider the impact of $R_{Z_0}$, the test limits may be set based on only $R_s$ and $R_L$. The nominal DC signal amplitude is only about 97% of the expected amplitude of $0.5V$. These losses due to the trace resistance $R_{Z_0}$ can come from any element in the path from the I/O buffers on the ATE to the I/O buffers on the UUT. Trace resistance on any PCB, including any traces on the ATE and UUT, is likely to contribute to a significant percentage of the total $R_{Z_0}$. Trace resistance is becoming a bigger and bigger problem because as board densities go up, the dielectric thicknesses get thinner. This forces the controlled impedance traces to also get thinner to maintain their given impedance. Using the following equation from [1, p.57]:

$$R_{DC} = \frac{1.669 \cdot 10^{-8} W \cdot T}{W \cdot T} \Omega/m$$

(2)

where $W$ and $T$ are respectively the width and thickness of the trace in meters, we can create the graph in Figure 2.

Using another equation from [1, p.57]:

$$R_{DC} = \frac{0.341 \cdot 10^{(AWG-10)/10}}{100} \Omega/m$$

(3)

where $AWG$ is the American wire gauge, we can create the graph in Figure 3. Since PCB traces are typically measured in mils rather than meters the units were converted accordingly for the plot. For example a 5mil wide trace made of $\frac{1}{2} oz$ copper has a trace resistance of about $2.3 \Omega/ft$. Therefore a $1 ft$ trace on $\frac{1}{2} oz$ copper would have a DC resistance of about $2.3\Omega$. These resistances can add up and quickly eat into the loss budget. Cables tend to be far less resistive per unit length than PCB traces but their resistance cannot be overlooked, especially for longer cables. Figure 2 shows resistance due to the cable which is measured in meters. As we can see, a $3m$ cable made of $30 AWG$ wire is far less resistive than a $1 ft$ long $5mil$ wide trace made of $\frac{1}{2} oz$ copper. Therefore it is important for the test engineer to refrain from using switch matrix cards that are constructed primarily of traces on a PCB.
for single ended signals must be made in setting up a differential test setup.

C. Characteristic Impedance and Mismatch

Impedance mismatch can reveal itself as signal amplitude loss, especially in cases where termination is only on one end of the transmission line. The following set of figures show a pulse response to three different termination schemes under two different mismatch conditions. The three termination schemes are:

- Voltage mode driver with source termination,
- Current mode driver with load termination, and
- Driver with source and load termination (double termination).

All transmission line simulations in this paper are performed using a single ended signal with nominal $Z_0 = 50\Omega$ unless otherwise noted. The same concepts can be applied to differential signals, since each element of the differential signal can be converted to a single ended signal. The simulations in this paper use rise times that are much faster than the data rate. The rise times are fast enough that their impacts on the simulations are negligible. If slower rise times are used, the user must compensate for them in his or her estimates. Transmitting data with slower edges will produce results that are worse than the performance discussed in the paper.

The two mismatch conditions evaluated in the following figures are:

- A 1pf capacitor to ground, representing a via or connector pin, two-thirds of the way between the transmitter and receiver, and
- Multiple cascaded transmission lines with impedance mismatches of $\pm20\%$ from the nominal trace impedance.

The discontinuities and mismatches were chosen to highlight the benefits of double termination.

Figures 4 and 5 both illustrate the benefits of using both source and end termination.

Impedance discontinuities in the transmission path can have a significant impact on the signal performance. The mismatches can negate the effects of a high performance cable.

![Figure 4. Simulation of various terminations with capacitive discontinuity in network](image1)

![Figure 5. Simulation of various terminations with impedance mismatch in network](image2)
D. Insertion Loss

Insertion loss is generally provided by high bandwidth cables and connectors for systems that are terminated on both ends. As the ATE is connected to the UUT through several interface connectors, adaptors, and cables, it is not obvious how the combined insertion loss coefficients affect the eye diagram of a multi-gigabit signal. From the prior section, we learned that much of the signal is preserved in a double terminated line. Further discussion about the benefits of termination at both ends can be found in [2]. For this reason, this section assumes that the system is double terminated as is the case for most multi-gigabit bus types like PCI Express [3]. When reflections are minimized, the multiple networks can quickly be cascaded by multiplying the insertion loss coefficients of each of the elements in the system [4]. If reflections are a significant concern, the s-parameters can not be cascaded through simple multiplication. They first must be converted to transmission parameters, or t-parameters. There is more on this topic in [4]. This paper focuses on the use of s-parameters, because they are more readily available from manufacturers of connectors, cables, and PCBs.

The Figure 6 shows the insertion loss of three transmission paths with negligible reflections. Path 1 acts like a signal filter that attenuates the signal frequency components at a rate of 1dB/GHz. Path 2 acts like a signal filter that attenuates the signal frequency components at a rate of 3dB/GHz. The combined plot shows the insertion loss of both paths cascaded. We know that in a well matched network with minimal reflections, the magnitude of the insertion loss of the full network is the product of the insertion loss of the individual parts, or the sum of the insertion loss of the individual parts when measured in decibels. Since the plots are displayed in decibels and the insertion loss is linear on the log scale, the cascaded network has a slope that is the sum of the individual paths. In this example, the frequency components of the cascaded network attenuate the signal at a rate of 4dB/GHz. Most cables do not have such a linear insertion loss profile. However, a test engineer however can make some piecewise linear estimates for the individual s-parameters to quickly get an idea of the overall insertion loss. This paper uses linear estimates for the transmission lines because good cables that are designed for multi-gigabit operation have very close to linear loss at the frequencies of operation.

![Insertion Loss Magnitude (dB)](image)

Quickly estimating the overall signal loss makes the test engineer much more efficient in determining the likely performance of the test setup. Properly simulating and evaluating all of the elements in the signal path in a test setup can be iterative and time consuming. The following sections offer techniques to help reduce the number of iterations and simulations a test engineer takes to establish a highly repeatable test.

E. AC Resistance – Skin Effect and Proximity Effect

An earlier section discussed the DC resistance of a trace and a wire. Unfortunately, at higher frequencies, the resistance of the conductor increases. Two contributors to this phenomenon are skin effect and proximity effect. Detailed discussion about these topics can be found in [1, pp.58-59]. The test engineer must understand that as frequencies increase, currents in the conductor tend to concentrate around the perimeter or “skin” of the conductor, thereby increasing the resistance of the path. Therefore, increasing the conductor thickness also increases the conductor perimeter which both lowers the DC resistance and the AC resistance.

The impact of skin effect and proximity effect are likely to be included in the s-parameter coefficients, because s-parameters coefficients of devices are typically measured, not simulated. The test engineer should confirm whether the s-parameter data from the manufacturer was measured or simulated. If it was purely simulated, the engineer should leave a little margin in their design budget to account for some additional loss.
F. DIELECTRIC LOSS

Dielectric loss becomes a major loss contributor in designs greater than 1 Gbit/s. Therefore, the choice of materials used in the construction of any cable or PCB becomes extremely important [1, pp. 184-221]. While skin effect on PCBs begins to dominate signal loss in the tens of megahertz range, dielectric loss begins to dominate at around 500 MHz [1, pp. 184-221]. The frequencies at which skin effect and dielectric loss dominate are different on coaxial cables as discussed in [1, pp. 220].

It is important to note that skin effect loss increases proportionally to the square root of the frequency while dielectric loss increases proportionally to frequency [1, pp. 184-221]. As a result, the dielectric loss becomes much more dominant than skin-effect loss in multi-gigabit designs.

III. DIAGNOSIS

The prior section identified several possible considerations for the test engineer. This section discusses techniques to help pinpoint problems within an existing network. The first step is to identify whether the signal loss is due to impedance discontinuities or insertion loss. Before we continue with this section, it is important to note that although an eye diagram is a great tool to get a summary of the signal performance, it is not a good tool to diagnose the likely cause of signal loss.

Let us look at Figure 7 as an example. It is far from obvious why the eye in each of the diagrams is closing. One may assume that given the choice between two options, that the eye in the top plot is closing due to insertion loss and that the eye diagram in the bottom plot is due to discontinuities in the transmission line, but there wouldn’t be any certainty.

Another option is to transmit signals from the ATE or UUT at a very slow data rate relative to the propagation delay through the interconnect path. That way the test engineer can observe the signal using an oscilloscope to determine whether the signal looks like the path has impedance discontinuities or is simply lossy. Once the test engineer identifies the reason for loss, the test engineer can improve the setup accordingly.

Figure 7. Simulated eye due to loss vs eye due to impedance discontinuities

One method to determine impedance discontinuities is to use a time-domain reflectometer (TDR) to determine any mismatches in the transmission path. Unfortunately, test engineers do not always have access to a TDR. And sometimes even if a TDR is available, there may not be an easy way of connecting into the path.

Figure 8. Simulated of a slow pulse through transmission path with impedance discontinuities

The following section discusses considerations to improve the signal.

IV. HOW DO I GET MY SIGNAL BACK

The previous sections showed why a test engineer must consider the entire signal path as a filter. The prior sections also discussed elements for the test engineer to consider when the engineer tries to preserve the signal. This section discusses improvements to the test setup that may help mitigate some of the signal losses.

A. Materials

Both the conductor and the associated dielectric have an impact on the signal amplitude. A thin conductor can adversely affect both the DC and AC signal. A poor dielectric can greatly affect the network’s AC performance. These parameters may be fixed on the ATE and the UUT, but the test engineer should consider using the best materials in all of the elements in the signal path between the ATE and the UUT. It may be very expensive to use the best materials, so the engineer may need to consider other options. One such option is emphasis.
B. Emphasis

There are many types of emphasis. Two commonly used terms are pre-emphasis and de-emphasis. The idea behind emphasis is to provide a better signal to noise ratio by increasing the signal amplitude during transitions compared to the signal amplitude when it is already at a given logic state. Pre-emphasis is applied by increasing the signal amplitude during logic state transitions. De-emphasis is applied by decreasing the signal amplitude after logic state transitions. The simulations and measurements in this paper apply emphasis for the entire unit interval on a transition bit. Non transition bits are de-emphasized. This is a common method used in high-speed differential bus standards such as PCI Express. De-emphasis is much more common than pre-emphasis because it is easier to implement in hardware.

1) Is More Emphasis Better?

Pre-emphasis and de-emphasis should only be used when needed. In a low loss environment, emphasis adds deterministic jitter because of the variance in the initial during transitions. Figure 9 shows two eye diagrams. The top eye diagram shows a low loss network output with no de-emphasis. The bottom eye diagram shows the same low loss network output with 6.89dB of de-emphasis.

Table 1 summarizes the eye diagram in Figure 9. In this case, both the peak-to-peak jitter and eye opening are better without de-emphasis. The eye opening is measured by the difference between the smallest logic high state and the largest logic low state in the middle of the eye. The peak-to-peak jitter is determined by the width of the midpoint crossing of the eye. There are no statistics applied to these numbers. Figure 10 shows simulations of similar eye diagrams in a higher loss network. This simulation models a physical test configuration with a Xilinx Vertex 6 FPGA driving about 8 inches of PCB etch going through 3 high bandwidth connectors and 3 meters of cable. Cascading insertion loss data provided by the cable and connector manufacturers with the simulated insertion loss of the PCB and remaining connector, we can approximate the path with a simple insertion loss profile that rolls off at about 4.3 dB/GHz. Figure 11 shows a scope shot of the actual setup using a Tektronix DSA71254 12.5GHz Digital Serial Analyzer using a 12.5GHz differential probe.
TABLE III. HIGH LOSS MEASUREMENT EYE-DIAGRAM SUMMARY

<table>
<thead>
<tr>
<th>Figure</th>
<th>Table Column Head</th>
<th>P-P Jitter (ps)</th>
<th>Eye Opening (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11. Top</td>
<td>No de-emphasis</td>
<td>170</td>
<td>318</td>
</tr>
<tr>
<td>11. Bottom</td>
<td>With 3.97 dB de-emphasis</td>
<td>113</td>
<td>438</td>
</tr>
</tbody>
</table>

Signal de-emphasis in a high loss network improves the jitter and eye-opening. It also reduces the overall signal amplitude as shown. Table 2 summarizes the eye diagrams in Figure 10 and shows a significant improvement to both the jitter and eye opening. Table 3 summarizes the eye diagrams in Figure 11 and shows a significant improvement to both the jitter and eye opening. The examples in figures 10 and 11 show that peak-to-peak jitter and the eye opening improve with de-emphasis. The simulation has an ideal source driving a cable in a noiseless environment with no crosstalk. The scope shot was taken in a system with many noise and crosstalk contributors. Furthermore, the scope shot includes far more samples than the simulations. So now that we know emphasis is appropriate in certain situations, how can one determine when and how much to use?

The optimal de-emphasis in the measurement above was determined empirically. The goal is to quickly determine the ideal de-emphasis to apply to a given network. The ideal amount may require many simulations and experiments, but a reasonable estimate may be sufficient and simpler to attain. Figure 12 shows two plots. The top plot shows the simulated eye opening versus de-emphasis of a 5Gbits/s pseudo-random bit stream (PRBS) for different interconnects. The bottom plot shows the simulated peak-to-peak jitter versus de-emphasis of a 5Gbits/s pseudo-random bit stream (PRBS) for different interconnects. The insertion loss profile for each of these interconnects is shown in Figure 13. Figure 12 shows that the eye opening is at a maximum at nearly the same de-emphasis setting as when the jitter is at a minimum. If we assume a logarithmically linear insertion loss as in Figure 13, we can find the optimal points in Figure 12 to approximate the proper de-emphasis setting with the following equation:

\[ G_{\text{emph}} \approx 0.575 \cdot L_{f_0} \]  

(4)

Where \( G_{\text{emph}} \) is the amount of de-emphasis in units of dB to apply and \( L_{f_0} \) is the insertion loss in units of dB at the frequency equal to one-half the data rate for a single data rate pattern set.

Figure 14 shows the benefits of applying the equation 4. The signal jitter and eye opening are greatly improved by applying the appropriate de-emphasis. The maximum signal datarate in this example is 5Gbits/sec so the fundamental frequency, \( f_0 = 2.5GHz \). If the insertion loss is rolling off the signal amplitude at 6dB/GHz, we can determine that \( L_{f_0} = 2.5GHz \cdot 6dB/GHz = 15dB \). Applying the formula in equation 4, we can determine \( G_{\text{emph}} \approx 0.575 \cdot 15dB = 8.625dB \) for a Gbit/sec datarate.
We can clearly see that the de-emphasis is most beneficial where there is more signal attenuation. As the bit interval increases, the fundamental frequency of the data-rate decreases, and therefore the total insertion loss decreases. The eye naturally opens with lower insertion loss, thereby reducing the benefit of adding de-emphasis.

Figure 15 translates the magnitude data from Figure 14. The solid line represents the loss in decibels defined by the insertion loss coefficients. With no de-emphasis, the eye opening drops below the solid black line at approximately -5.5dB and then begins to quickly roll off after about -8dB.

With the calculated de-emphasis applied to the system, the eye opening amplitude continues to stay above the solid black line past -14dB. Therefore the system insertion loss coefficient at $f_0$ may be a reasonable guide as to the likely eye opening at the receiver when applying the calculated de-emphasis.

It is important to understand that these simulations were performed using a rise time that is one tenth the unit interval. If the test engineer wants to approximate system behavior with a slower edge, they may want to identify the insertion loss coefficients at $f_0$ that would reduce the rise time of a step to the rise time the buffer can produce. Once this insertion loss is identified, it can be cascaded with the rest of the network to provide a better estimate.

Let us check the validity of this equation 4 using the example with the Xilinx FPGA driving 3 meters of cable. The path loss was estimated to degrade the amplitude by $4.3dB/\text{GHz}$. Using equation 4, we estimate that the programmed de-emphasis should be about $3.86dB$ when operating at $3.125GBits/sec$. The FPGA de-emphasis setting that produced the best results was $3.97dB$.

If we want to pass a $2.5GBits/sec$ PRBS through the same network, we can expect that the optimal de-emphasis setting should be about $0.575 \times 5.375dB = 3.09dB$. The closest programmable option in the FPGA is $3.08dB$. Figure 16 and table 4 show the results of this experiment.

<table>
<thead>
<tr>
<th>Table Column Head</th>
<th>Figure</th>
<th>Emphasis</th>
<th>P-P Jitter (ps)</th>
<th>Eye Opening (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16. Top</td>
<td>No de-emphasis</td>
<td>196</td>
<td>359</td>
<td></td>
</tr>
<tr>
<td>16. Middle</td>
<td>With 3.08 dB de-emphasis</td>
<td>146</td>
<td>445</td>
<td></td>
</tr>
<tr>
<td>16. Bottom</td>
<td>With 6.89 dB de-emphasis</td>
<td>164</td>
<td>322</td>
<td></td>
</tr>
</tbody>
</table>
Table 4 shows that using the calculated de-emphasis for the setup produces the lowest jitter and biggest eye opening. Because there is not much overshoot, the initial conditions have very little variance and therefore produce the lowest jitter and the largest eye height.

The test engineer should try to obtain test equipment that supports programmable de-emphasis at the ATE’s front end. The test engineer should consider other loss contributors, such as signal and system noise and crosstalk. Further material on crosstalk can be found in [1, pp.319-328] and [5, pp.189-221]. Margin must be built into the design to allow for their impact on the eye opening. Additional detail on the physics of transmission lines can be found in [6, pp.272-384].

V. LIMITATIONS

The simulations and data generated in this paper use simplified transmission line models and computations in the interest of providing reasonably accurate data to explain the concepts. The simulations do not account for system noise or crosstalk. They also do not account for system clock jitter. The goal is to provide the test engineer a reasonable estimate when determining the system loss budget. More elaborate simulations may provide more accurate data, but may be much more time consuming.

VI. CONCLUSION

The test engineer should consider a wide variety of options when setting up a test for a multi-gigabit per second bus. Conductor thickness impacts both DC and AC resistance, and therefore should be considered when designing the test setup. Impedance discontinuities can reduce AC performance dramatically. Having one uniform controlled impedance cable between the ATE and UUT is much more desirable than multiple cables with adapters and switches. The dielectric material used in the cable or any other interconnect path must be chosen to minimized dielectric loss. The programmable parameters available during the test such as pre-emphasis and de-emphasis may also be used to improve the signal quality through the transmission path. Any path from the ATE to the UUT is a giant filter, but a test engineer can minimize its impact on the signal with an understanding of some of the signal loss contributors mentioned in this paper.

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REFERENCES