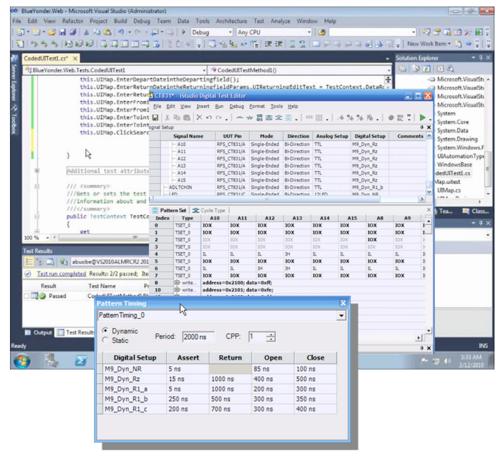
Teradyne eDigital HSSub App

General Purpose Parallel I/O for Digital Test

The eDigital HSSub App configures High Speed Subsystem (HSSub) Runtime Defined Instruments to perform general-purpose, stored pattern digital testing. This HSSub App and Instrument combination provides a high performance, cost effective solution for the parallel I/O requirements of recent weapon system designs. Multiple instruments can be can be combined to provide hundreds of synchronized bidirectional channels, or operate asynchronously to test independent UUT timing domains.



Overview

The eDigital HSSub App provides flexible parallel I/O capability that is vital for multiple generations of weapon systems. Even as copper or optical serial buses reduce the high UUT signal count of traditional I/O, critical parallel ports and discrete signals remain. Broad ranges of signal requirements demand a flexible, general-purpose capability for data and timing control. Rather than previous wide-range voltage demands, recent designs focus on a few standard logic levels such as LVTTL, LVDS, and some legacy TTL.

The eDigital HSSub App configures 6020-Series HSSub Runtime Defined Instruments to perform traditional truth table digital testing, where a sequence of stimulus and expected response patterns are stored in memory behind each of many bidirectional I/O pins. The eDigital HSSub App is invoked from a modern IVI-compliant C/C++/C# instrument driver that uses methodology similar to the M9/Di-Series instruments, familiar to thousands of TPS developers. Interactive graphical programming and debugging are supported with the iStudio eDigital Test Editor.

Key features include per-pattern control of logic state and directionality at speeds to 25 MHz, real-time hardware pass/fail processing, multiple data formats, at-speed timing changes, flexible looping, fine timing resolution, and low inter-channel skew. Additionally, the HSSub architecture provides new capabilities such as very deep local memory and very high bandwidth for efficient pattern loading with the option to move massive test results to the

Features

- High performance, general purpose, stored pattern parallel digital I/O capability
- eDigital HSSub App configures flexible, cost effective Runtime Defined Instruments
  - -HSSub-6020 LVTTL IO Instrument
  - -eDigital-6020A Instrument
- TTL, LVTTL, and LVDS support to 25 MHz with per-pin precision timing and very deep memory
- Hardware and programming architecture similar to ubiquitous L-Series systems and M9/Di-Series instruments

computer for post-test analysis. These capabilities streamline data-intensive tests for the latest designs that include processors, memory, and programmable logic.

As with all Teradyne Defense and Aerospace products, these capabilities are backed by a proven track record of superior long-term technical and logistics support.

eDigital HSSub App Specification Overview	
Supported HSSub Instruments	eDigital-6020A and LVTTL IO Expansion Instrument
I/O Signal Types (all channels)	1.8V, 2.5V, 3.3V LVTTL, or LVDS; 5V TTL-tolerant (eDigital-6020A only)
LVTTL channel count per instrument	64 static channels or 32 dynamic + 32 static
LVTTL channel count per subsystem	512 dynamic or static channels plus 512 additional static channels (16 instruments)
LVDS channel count per instrument	32 differential LVDS pairs
LVDS channel count per subsystem	512 differential LVDS pairs (16 instruments)
Static test operation modes	Immediate single-pattern execution or with programmable delay
Static stimulus to response delay	100 ns to 6.5536 ms
Dynamic test operation	Multiple stimulus & response patterns in local memory of multiple channels
Dynamic data rate	2.543 KHz to 25MHz (393 us to 40 ns period)
Data formats	NRET, RONE, RZERO, ROFF
Per-pattern Channel Opcodes	IOX (drive off, detector ignored) IH & IL (drive 1/0) MH & ML (drive 1/0, expect same) IHOL & ILOH (drive 1/0, expect opposite) OH & OL (expect 1/0) Keep & Toggle (maintain or complement the previous state)
Pattern Memory Depth	8M (each containing one of the channel opcodes)
Results Memory Depth	12M
Looping	Counted or conditional on real-time hardware state
Stimulus timing control	Two edges per pattern, each with 1ns resolution, independent per channel
Response timing control	One comparison edge with 1 ns resolution, independent per channel
Timing sets	256 timing definitions selected by the pattern
Minimum pulse width	5 ns
Stimulus & response edge accuracy	+/- 3 ns