

## Di-Series Digital Test Instruments

### Versatile C-size VXI Instrument for Defense and Aerospace Applications

Teradyne's Di-Series Digital Test Instruments (DTI) pack the industry's most powerful combination of performance, density, flexibility, usability, and reliability into a highly integrated, standards-based solution. The Di-Series DTI increases usability, functionality and commonality while reducing the total number of instruments needed by a test system. As a result, using Di-Series instruments decreases a test systems footprint, programming, support, and cost-of-ownership. As part of Teradyne's Core System Instrumentation (CSI) portfolio, the flexibility and performance of Di-Series instruments meet the essential requirements common to Defense and Aerospace automatic test equipment (ATE). In addition, Di-Series instruments provide the key features needed to test all levels of integration from the board level (SRA/SRU) to box level (WRA/LRU).



#### The Digital Test Heritage

The Di-Series instruments build upon Teradyne's digital test success first established by the L-Series functional testers and the M9-Series DTIs. Like the M9-Series, the Di-Series instruments use VXI-compliant hardware and software for easy integration with other instruments in standard C-Size VXI-based test systems. Backward compatibility preserves prior hardware and software test investments.

#### Field Proven Success

Many of the world's leading defense and aerospace factories, depots, and intermediate-level test facilities rely on Teradyne's DTI. Our instruments are used in a wide range of applications, including the U.S. Department of Defense (DoD) Standard automatic test system (ATS) Families including U.S. Marine Corps VIPER/T (TETS), U.S. Army NGATS (IFTE), Navy eCASS (CASS FoT), and RTCASS testers. Teradyne's digital instruments also form the core of the Air Force VDATS and Teradyne Spectrum 9100 avionics testers associated with key fighter, bomber, cargo, and missile programs. The CSI family, including the Di-Series, is a key element of the Agile Rapid Global Combat Support (ARGCS) Advanced Concept Technology Demonstration whose success is helping to modernize future DoD ATS families.

#### Commitment to Technology

Defense and aerospace test engineers face an array of difficult test challenges that include:

- Upgrading or replacing aging test systems and maintaining compatibility with legacy equipment
- Building equipment to test multiple stages of assembly
- Preparing for next-generation platforms
- Managing the entire test development process despite ever-increasing complexity

#### Key Features

- Proven Teradyne Compatibility maintains test program set (TPS) investment with previous generations of Teradyne digital instrumentation and systems
- LRU/WRA-Centric Flexibility addresses diverse requirements; units under test (UUTs) from boards to boxes, old and new designs, legacy instrument replacement
- Unmatched Performance addresses the latest technology and provides the best quality of test
- Breakthrough Usability provided by flexible hardware and innovative development and debugging software
- Reliability, Survivability and Supportability that keeps systems running based on decades of Defense and Aerospace experience

#### Capabilities

- 64 single-ended 50 MHz channels
- Per-channel programming of levels & timing
- 256K flexible pattern memory per channel
- 8M Deep Serial Memory per channel
- Handshake engine for asynchronous busses
- iStudio graphical development & debug tool

The Di-Series DTI includes the following features and benefits that address these issues.

## 1. Proven Teradyne Compatibility

The digital sections of an L-Series or CASS test program set (TPS) can be translated to operate with Di-Series instruments using Teradyne's proven TPS Converter Studio™ software. The converter generates C-language code that controls the Di-Series instruments through the Teradyne copyrighted CShell™ Applications Programming Interface featuring function calls similar to L-Series language statements. The Di-Series instruments feature per-channel levels and timing control to allow easy and conflict-free mapping from L-Series to Di-Series. Programs previously written for the M9-Series DTI will run directly on Di-Series instruments. Programs that used the CShell API with the M9-Series instruments may now control the Di-Series without code changes. Programs that directly called the M9-Series VXIplug&play driver can also use the Di-Series instruments. By replacing the M9-Series driver at run time, the Di-Series software provides full binary compatibility, allowing the typical M9-Series TPS to run without recompilation or linking. In addition, the Di-Series iStudio software can convert M9-Series tests into native Di-Series code so the TPS developer can take full advantage of new Di-Series functionality.

## 2. WRA/LRU-Centric Flexibility

Boxes (WRA/LRU) require numerous bus-oriented tests that involve asynchronous transfers. The Di-Series instruments feature a new Handshake Engine that simplifies asynchronous data transfer based on the UUT response. The Handshake Engine is simple to program, eliminates complex multi-pattern homing loops that determine when the UUT is ready, and reduces latency. Other instruments generally lack the ability to easily and quickly interact with a UUT. The Di-Series overcomes this limitation and addresses the requirements of all levels of assembly from board to box. This flexibility improves the quality of test and reduces programming costs. Most boxes have multiple I/O ports that operate concurrently, with no discernable common timing. Until now, TPS developers either had the difficult task of sharing a single instrument across the ports, or were forced to equip systems with multiple, expensive digital instruments. A unique feature of the Di-Series is its programmable partitioning that provides multiple, independent virtual instruments that operate concurrently, but totally asynchronously from one another. Each virtual instrument can address one port and improve operational test quality while reducing the development effort.

Newer UUT designs require increasingly larger quantities of test data. The Di-Series Deep Serial Memory can efficiently address the problems associated with loading, unloading, and testing large blocks of test data, testing memory, or configuring a box. Each Di-Series channel has 8 M locations of sequentially addressable data memory to complement the 256K of dynamic pattern memory that manages the repetitive control operations. Since the Deep Serial Memory is behind every channel, bus widths can range from narrow serial to wide parallel buses.

The Di-Series recognizes that the signal transmission path between

the tester and UUT can be demanding. For instance, the same channel that supports the small voltage swings associated with Low-Voltage Differential Signaling (LVDS) on one TPS can support 30 V swings associated with legacy I/O requirements of another TPS. LVDS features programmable edge speeds: slow edges to avoid overshoot, undershoot, and ringing in uncontrolled situations; or fast edges for high accuracy and performance in a controlled environment. With independent, per-channel programming of edge speeds, the Di-Series can greatly simplify TPS debugging, optimize TPS quality, and improve repeatability.

## 3. Unmatched Performance

Emerging designs increasingly use differential pairs to permit higher speed I/O despite several feet of cabling. The latest designs use LVDS and legacy designs often contained in earlier forms of differential logic that present significant test challenges. The Di-Series channels can be paired to accommodate differential signals that avoid specialized test instruments or additional circuitry in the test adapter.

Teradyne's Di-Series instruments can simultaneously test the differential logic state and the common mode offset that the pair shares with optimal edge speeds and line termination. Combining LVDS and 50 MHz capability provides a practical means to provide high-performance signals in a real-world test environment.

The Di-Series employs QuadDetect™ to more comprehensively test digital logic states. Other vendor instruments typically use dual-threshold detectors: one to ensure a minimum logic "1" and another to ensure a maximum logic "0." QuadDetect uses four detectors to band the lower and upper limits of each logic state to improve the quality of test and decrease the No-Fault Found escape rate.

## 4. Breakthrough Usability

The Di-Series hardware was designed to maximize usability by eliminating shared resources. Now, instead of programming the drive, detect, and load parameters in a limited number of sets, each Di-Series channel can be programmed independently. Instead of sharing a small number of drive phases and test windows, each Di-Series channel has an independent phase and window. And, each channel has independent control over driver edge speed. Channel independence allows engineers and technicians to focus on the UUT rather than the limitations of the test system, whether programming, debugging, or troubleshooting.

As digital tests become more complex, the creation and debugging of tests can become expensive. The Di-Series is backed by iStudio, a comprehensive graphical development and debugging environment that complements existing Applications Development Environments (ADEs) and test executives. iStudio features a Digital Test Editor for codeless programming; visualizing and editing the timing, levels, and patterns that comprise a digital test. iStudio can be used interactively on the test system, or can be used on a stand-alone computer with instrument simulation. A completed test can be exported as a data file, reloaded into the instrument, and executed under control of the TPS using any language. Alternatively, the Digital Test Editor can export the test for enhancement in standard languages (C or C#) for use in tools such as LabWindows™ or Visual Studio™. iStudio will



## Specifications

Parameter	Value
Data and clock rate	25 MHz (Di-025 models) or 50 MHz (Di-050 models)
Channels/VXI slot	64 single-ended (32 differential pairs) OR 32 single-ended (16 differential pairs)
Dynamic pattern memory	256K patterns
Deep serial memory	8 M per channel, sequentially accessed
Timing sets	256
Pattern branching	Loops, branches, conditionals, subroutines, event handlers
Algorithmic capabilities	CRC generation, keep & toggle, Teradyne L-Series compatible MemTest
Synchronization and debugging capabilities	Programmable handshake, external trigger-in, external trigger out, external clock in & out, test envelope (burst running signal), VXI TTL trigger bus, dynamic breakpoints
External clock synchronization	DC to 50 MHz

Parameter	Value
Drive phases/test	Independent phase & window per channel windows
Drive phase/test window resolution	1 ns
Drive and detect skew	±3 ns max across all channels
Minimum pulse width	10 ns
Channels per cage	768
Virtual instruments/cage	24 maximum
Drive current	Up to 80 mA with programmable limits
Drive & detect levels (15 V models)	-5 V to +15 V OR -15 V to +5 V, 20 V max swing
Drive & detect levels (30 V models)	±30 V, 30 V max swing
Over-voltage protection	Automatic relay disconnect within 50 $\mu$ s
Data formats	Seven (NR, R0, R1, RZ, RC, RM, SC)
Driver slew rate control	100:1 adjust range per channel, 1 V/ns maximum
Guided probe	Optional
Operating range	0 – 50°C ambient